

## Wideband Transmit-Receive Digital Signal Processors

Check for Samples: [GC5330](#), [GC5337](#)

### FEATURES

- Integrated Transmit and Receive Digital IF Solution
- Up to 4 TX, 8 RX, Plus DPD Feedback
- TX-Transmit Includes DUC, CFR, DPD, TX Equalizer, and Bulk Upconverter
- 62-MHz TX Signal Bandwidth With Fifth-Order DPD Correction
- CFR: 6-dB PAR for WCDMA, 7-dB LTE Signals With EVM Meeting 3GPP Specs; Configurable for All Major Wireless Infrastructure Standards
- DPD: Memory Compensation, Typical ACLR Improvement of 20 dB or More
- RX-Receive Includes DC-Offset Cancellation, Front-End and Back-End AGC, Bulk Downconverter, RX Equalizer, I/Q Imbalance Correction, DDC
- 4 DDUCs, 1–12 Channels per DDUC, Each DDUC Can Be Programmed to TX or RX, at a Common Resampler Rate – Multimode Support
- Seamless Interface to TI High-Speed Data Converters
- 4 TX Aggregate Output to DACs up to 930 MSPS Complex
- 8 RX Aggregate Input From ADCs up to 1.24 GSPS Real
- Supports Envelope Tracking Techniques
- 16-Tap (Complex) RX Equalizers
- Two 4K Complex Word Capture Buffers for Signal Analysis, Adaptive Filtering, and DPD Algorithms
- TMS320C6748 DPD Optimization Software
- 1.1-V Core, 3.3-V I/O CMOS, 1.8-V I/O LVDS
- Power Consumption, 3.5 W Typical
- 484-Ball TE-PBGA Package, 23 mm × 23 mm

### APPLICATIONS

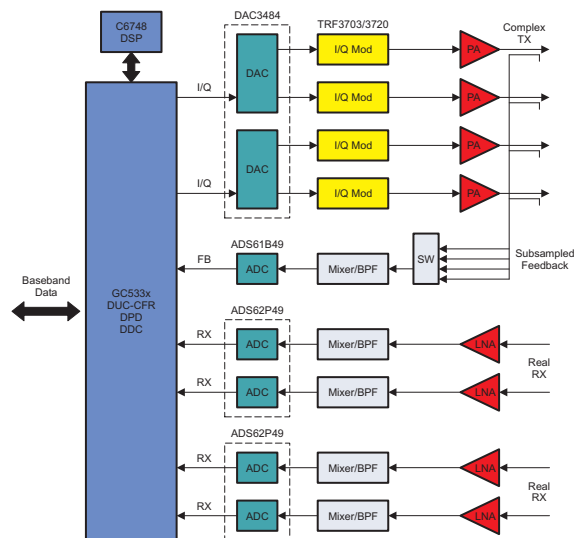
- Multi-Standard Base Stations
- 3GPP (LTE, W-CDMA, TDS-CDMA)
- MC-GSM
- WiMAX and WiBro (OFDMA)
- Multi-Carrier Power Amplifiers (MCPAs)
- Wireless Infrastructure Repeaters
- Up to 4 × 4 MIMO

### DESCRIPTION

The GC533x is a wideband transmit and receive signal processor that includes digital downconverter / upconverter (DDUC), transmit, receive, and capture buffer blocks. The transmit path includes crest factor reduction (CFR), digital predistortion (DPD) and associated feedback path, complex equalization, and bulk upconversion.

The receive path includes wideband and narrowband automatic gain control (AGC), bulk downconversion, complex equalization, and I/Q imbalance correction.

The DDUC section consists of four identical DDUC blocks, each supporting up to 12 channels. Each channel has independent fractional resamplers and NCOs to enable flexible carrier configurations. Multi-mode/multi-standard operation can be supported by configuring the individual DDUC blocks to different filtering and oversampling scenarios.



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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## DESCRIPTION (Continued)

The CFR block reduces the peak-to-average ratio (PAR) of the digital transmit signals, such as those used in third-generation (3G) code division multiple access (CDMA) and orthogonal frequency-division multiple-access (OFDMA) applications.

The DPD path with a 310-MHz DPD clock can be configured to support one antenna at 62 MHz, two antennas at 62 MHz each, or four antennas at 31 MHz each, all with an associated 5× DPD expansion bandwidth. The GC533x DPD processor reduces power amplifier (PA) nonlinearity, e.g., as measured by adjacent-channel leakage ratio (ACLR), by over 20 dB. By reducing the PAR of the digital signal and the PA nonlinearity, the operational efficiency of follow-on power amplifiers can be substantially improved.

A higher DPD bandwidth is possible with reduced DPD performance. Several architectures that provide performance and cost optimization are listed in [Table 1](#).

**Table 1. Sample Configurations for GC5330 {GC5337}**

| Figure                   | TX Antenna    | DPD Bandwidth | ET Support          | Feedback                   | RX Antenna                                 | Other                                                                   |
|--------------------------|---------------|---------------|---------------------|----------------------------|--------------------------------------------|-------------------------------------------------------------------------|
| <a href="#">Figure 1</a> | 2-62 {74} MHz | 310 {370} MHz |                     | Subsampled real            | 2 typical at 250 Msps, up to 4 at 250 Msps | Lower-cost 2-antenna solution                                           |
| <a href="#">Figure 2</a> | 2-62 {74} MHz | 310 {370} MHz |                     | Full-rate real up to 1Gsps | 2 at 250Msps, 4 with lower-rate RX ADC     | 2-antenna solution with full-rate real feedback                         |
| <a href="#">Figure 3</a> | 2-62 {74} MHz | 310 {370} MHz |                     | Subsampled complex         | 2 at 250Msps, 4 with lower-rate RX ADC     | 2-antenna solution with complex feedback, lower subsampling ratio       |
| <a href="#">Figure 4</a> | 2-62 {74} MHz | 310 {370} MHz | 2-envelope tracking | Full-rate real up to 1Gsps | 2 at 250Msps, 4 with lower-rate RX ADC     | 2-antenna solution, with envelope tracking with full-rate real feedback |
| <a href="#">Figure 5</a> | 4-31 {37} MHz | 155 {185} MHz |                     | Subsampled real            | 4 at 250Msps, 8 with lower-rate RX ADC     | Lower-cost 4 antenna solution                                           |

## ANTENNA MODE EXAMPLE DIAGRAMS

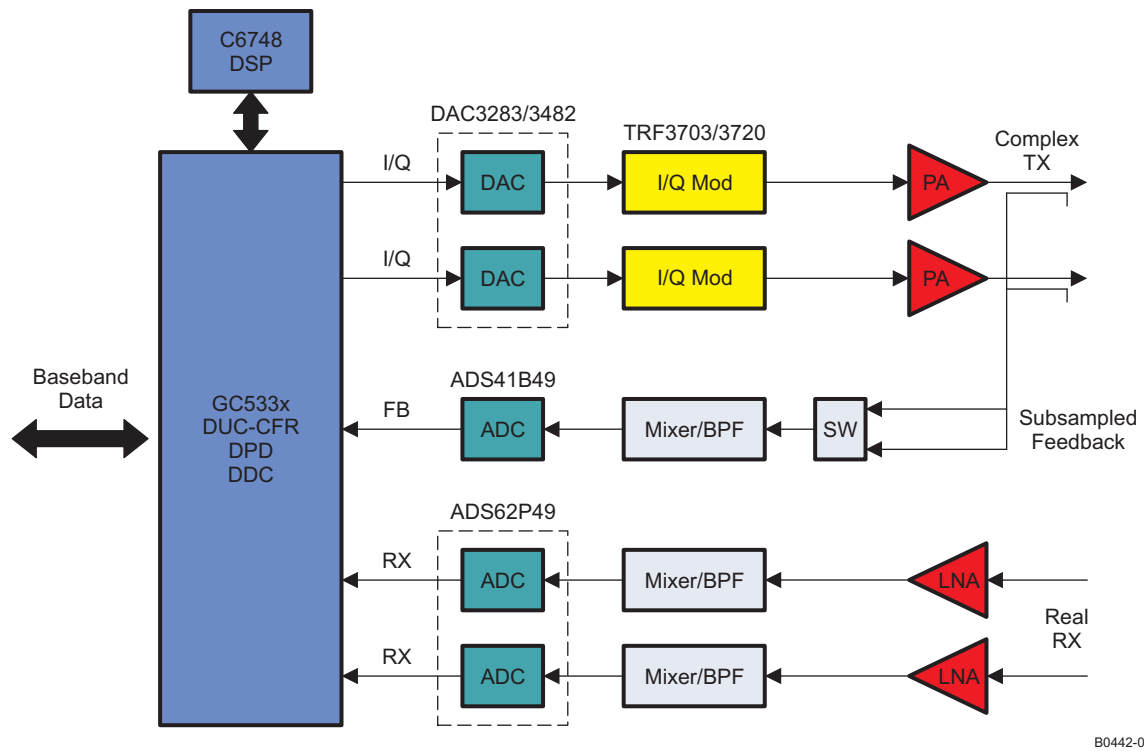


Figure 1. Two-Antenna-Mode Subsampled-Feedback Diagram

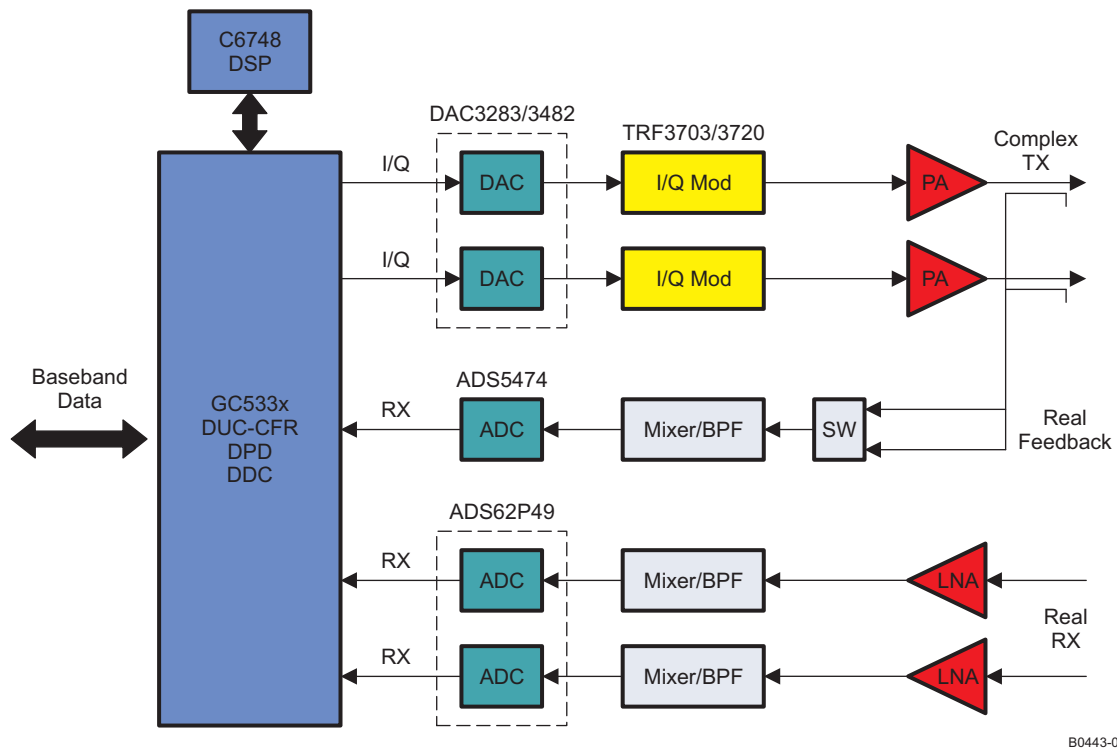
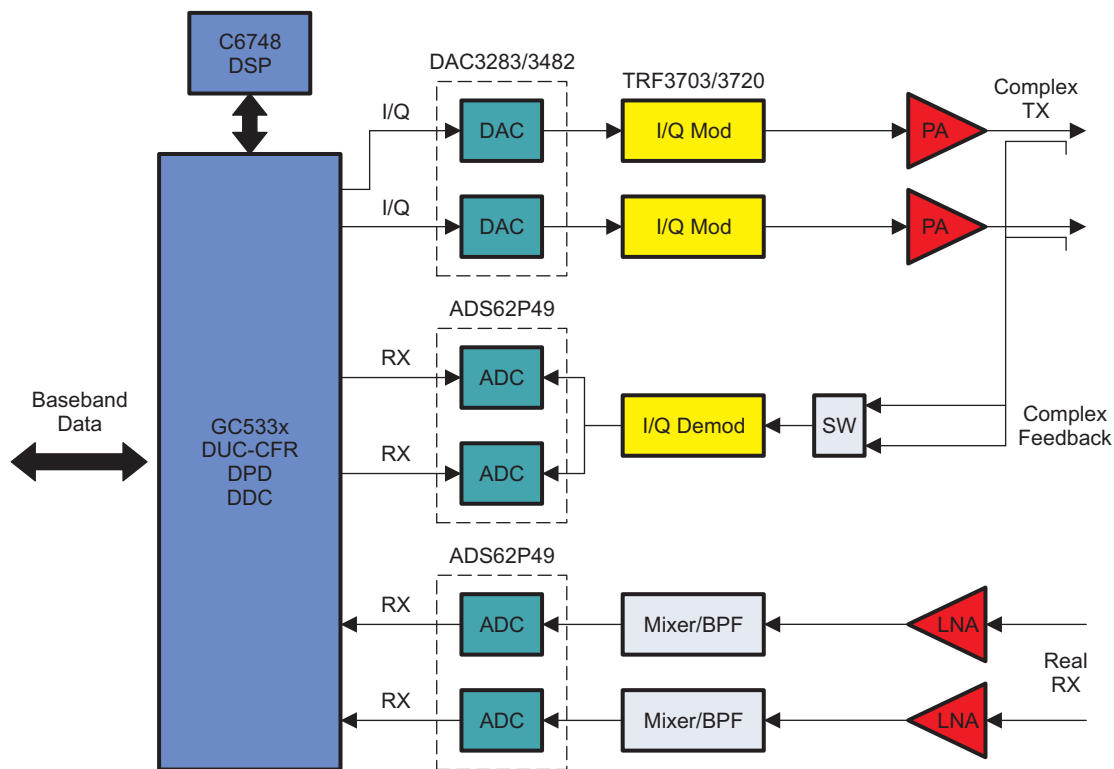
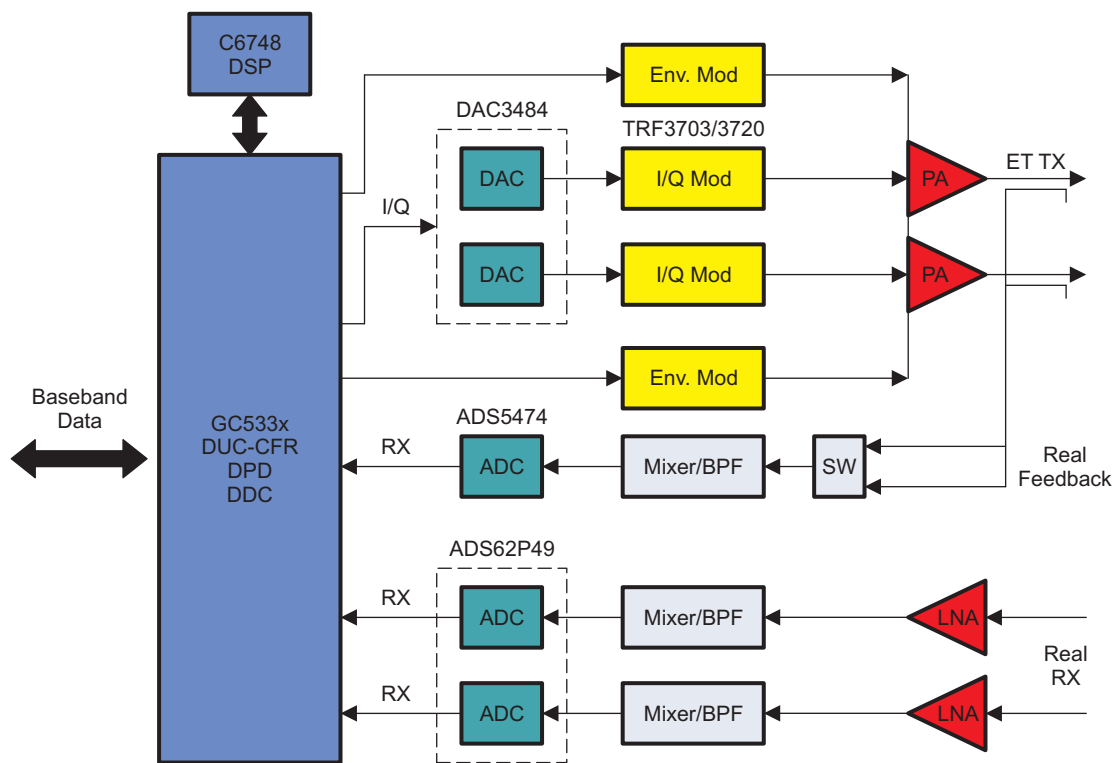


Figure 2. Two-Antenna-Mode Full-Rate Real-Feedback Diagram



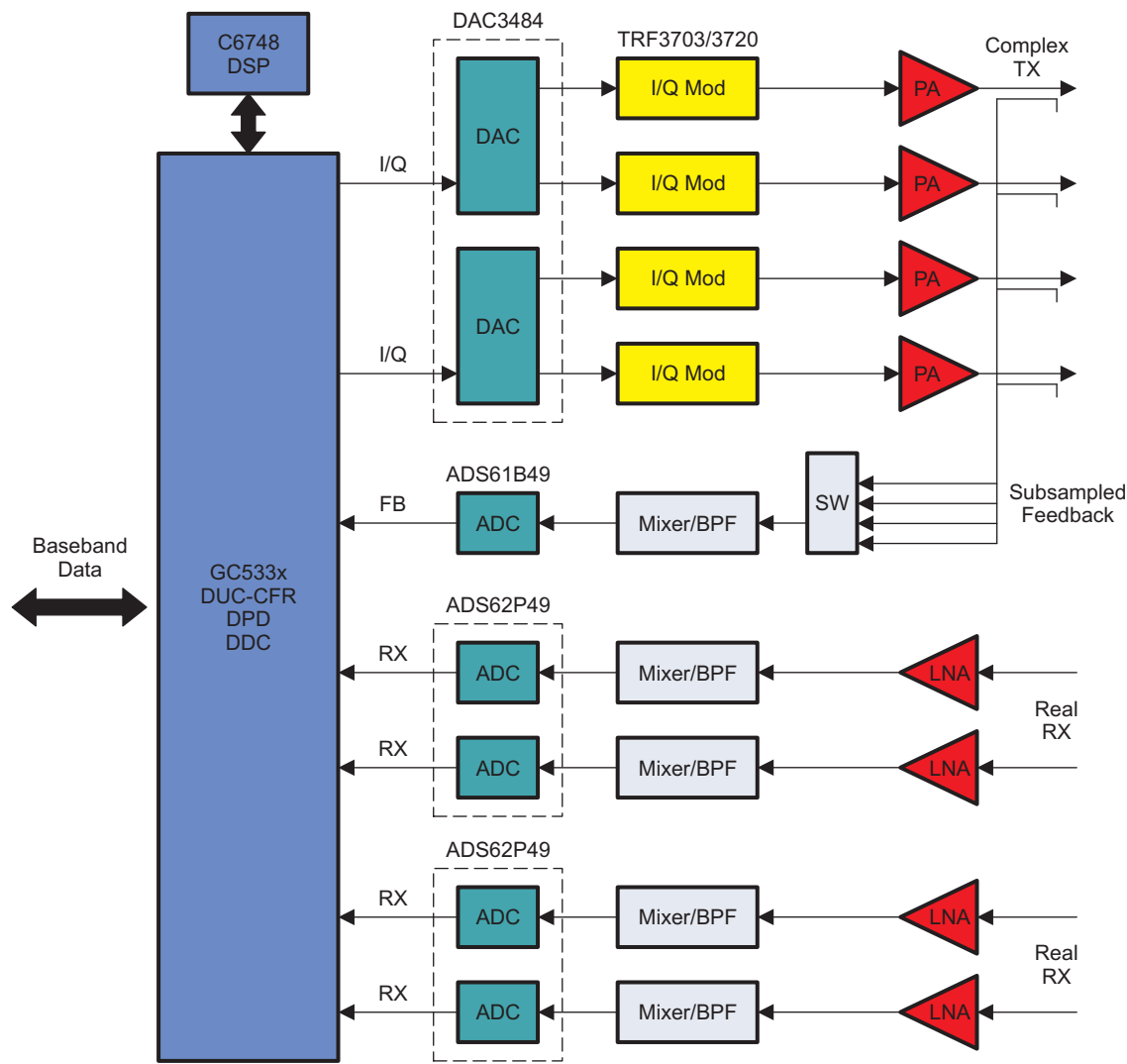
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Figure 3. Two-Antenna-Mode Complex-Feedback Diagram



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Figure 4. Two-Antenna-Mode, Envelope-Tracking, Full-Rate Real-Feedback Diagram



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Figure 5. Four-Antenna-Mode Subsampled Real-Feedback Example Diagram

## GENERAL DESCRIPTION

The GC533x is a wideband transmit and receive signal processor that includes digital downconverter/upconverter (DDUC), transmit, receive, and capture buffer blocks. The transmit path includes crest factor reduction (CFR), digital predistortion (DPD) and associated feedback path, complex equalization, and bulk upconversion. The receive path includes wideband and narrowband automatic gain control (AGC), bulk downconversion, complex equalization, and I/Q imbalance correction. The GC5337 is a higher-speed version of the GC5330 that has the same package, but with interfaces that can provide more processing performance for higher-bandwidth applications. In the descriptions, the GC5337 differences are shown with { } values.

The architecture supports different RX, TX, and feedback modes of operation. This provides for many configurations to optimize performance and cost.

- RX – real or complex input
- TX – real, complex, complex with envelope tracking
- Feedback – subsampled real, full-rate real, full-rate complex

The RX path can be configured for one or two multichannel ADC input ports. The RX block provides each ADC channel with a front-end AGC, IQ demodulation correction, real-to-complex conversion, complex mixing, decimation, and complex equalization. The RX block output is input to the DDUC block. The output of the DDUC block goes through gain and back-end AGC and is formatted for the baseband output.

There are four DDUC blocks. Each can be used for the RX DDC downconversion or TX DUC upconversion, one at a time. The DDUC has a complex mixer, cascade integrator comb filter, resampler, and a programmable FIR filter. Each DDUC can support 1 to 12 channels.

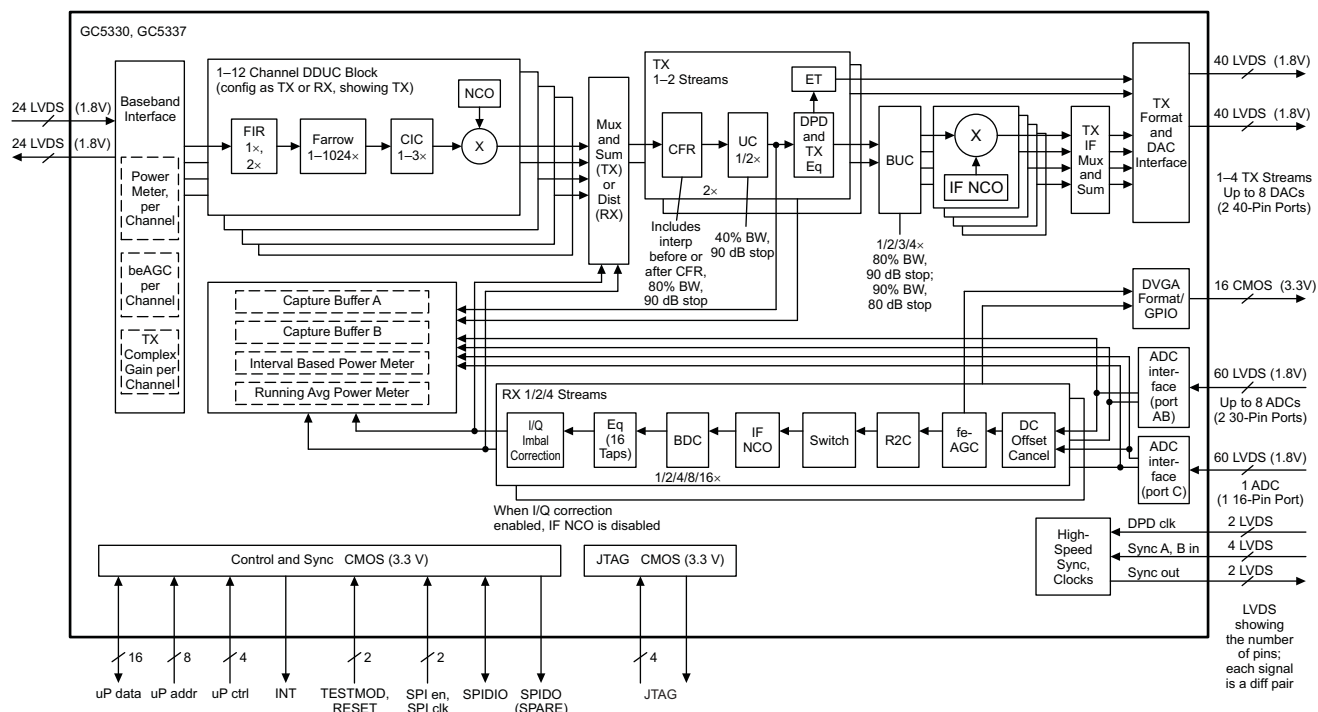
The TX path can be configured for one, two, or four antenna streams. In addition, with one or two antenna streams, an envelope modulator output is available. The DAC and envelope modulator share the same output ports. The TX input is from the baseband input, through the DDUC to create complex antenna streams. The CFR block provides for gain adjustment, peak reduction, and peak limiting. The CFR block peak power reduction and follow-on circular limiter provide the headroom to apply the DPD correction, and to lower the peak power results for more power amplifier efficiency. Additional interpolation stages after CFR expand the antenna stream bandwidth to the DPD bandwidth.

The DPD has both high-performance (more correction) and high-bandwidth (more bandwidth) modes. The high-bandwidth mode supports 62 MHz {74 MHz} for one or two antenna streams, and 31 MHz {37 MHz} for four antenna streams with fifth-order expansion bandwidth. The high-performance mode supports one antenna at 62 MHz {74 MHz}, two antennae at 31 MHz {37 MHz}, or four antennae at 15.5 MHz {18.5 MHz}. The GC533x DPD processor provides phase correction, gain correction, and nonlinear feedforward correction for each TX stream. The spectral emission or ACP performance is improved by 20 dB or more.

Specialized capture logic collects the RX input, feedback input, RX output, DPD input, and DPD output for the DSP processor to perform the adaption algorithm. The capture logic can also be used for performance monitoring and power measurement.

#### AVAILABLE OPTIONS

| PART NUMBER | T <sub>C</sub> | PACKAGE                     | THERMAL PROPERTIES                |
|-------------|----------------|-----------------------------|-----------------------------------|
| GC5330IZEV  | –40°C to 85°C  | 484 ball 23-mm × 23-mm PBGA | Heat transfer through package top |
| GC5337IZEV  | –40°C to 85°C  | 484 ball 23-mm × 23-mm PBGA | Heat transfer through package top |



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NOTE: UC1 and UC2 are for CFR interpolation; UC2 can only be used if UC1 is also used.

Figure 6. GC533x Block Diagram

## GC533x Introduction

The GC533x is a flexible transmit and receive digital signal processor that includes receiver and transmitter blocks, digital downconverter / upconverter (DDUC) blocks, crest factor reduction (CFR) and digital predistortion (DPD) engines, flexible LVDS data converter and baseband interfaces, and capture buffers for DPD and adaptive filtering algorithms.

Each of the four DDUC blocks can be configured as either a digital downconverter (DDC) or a digital upconverter (DUC). Typically, a system can be implemented as both TX and RX, with both DDC and DUC functions. The DDUC blocks provide programmable FIR filters with flexible numbers of taps, depending on signal bandwidth and number of channels, as well as fractional resamplers, CIC filters, and complex mixers. The DDUC complex mixers support static or hopping tuning functions.

beAGC after the DDC is part of the baseband interface. Static gain is applied in the BB block for both the DDC output and DUC input.

The receiver block provides dc offset correction, front-end AGC, real-to-complex conversion, complex mixing, decimating filters, a complex equalizer, and a blind RX IQ imbalance correction function.

The CFR block reduces the peak-to-average ratio (PAR) of complex, arbitrary TX signals. Reducing the PAR of the TX signal allows wireless-infrastructure (WI) base stations and repeaters to use smaller and lower-cost multi-carrier power amplifiers (MCPAs).

The DPD block can process one or two TX streams at 62 MHz {74 MHz} or four TX streams at 31 MHz {37 MHz} each, with fifth-order nonlinear correction. The DPD engine uses a companion TI DSP TMS320C6748 to collect the reference and feedback data, calculate the feedforward correction, and update the GC533x registers.

In WI applications, the GC533x meets multi-carrier 3G and 4G performance standards (PCDE, composite EVM, and ACLR) at PAR levels down to 6 dB for WCDMA and 7 dB for LTE, and improves the ACLR by over 20 dB at the PA output. The GC533x integrates easily into the transmit/receive signal chain between Texas Instruments' high-performance data converters and baseband processors such as the TI TMS320C64xx family. In wireless repeater applications, the GC533x can provide seamless interfaces to TI data converters, along with receive and transmit filtering, DDC, and DUC functions.

The GC533x is extremely flexible and can be used in system architectures with different signal types and TX-by-RX antenna configurations such as 2×2, 2×4, 4×4, and 4×8.

The GC533x EVM system provides an example sector transmit-receive signal chain solution, from the multi-carrier baseband to the RF antenna.

## ABSOLUTE MAXIMUM RATINGS

over recommended operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

|                    |                                   | MIN                                                              | MAX                      | UNIT |
|--------------------|-----------------------------------|------------------------------------------------------------------|--------------------------|------|
| V <sub>DD</sub>    | Core supply voltage               | −0.3                                                             | 1.32                     | V    |
| V <sub>DDA</sub>   | PLL analog voltage                | −0.3                                                             | 2                        | V    |
| V <sub>DDS</sub>   | Digital supply voltage for TX     | −0.3                                                             | 2                        | V    |
| V <sub>DDSHV</sub> | Digital supply voltage            | −0.3                                                             | 3.6                      | V    |
| V <sub>IN</sub>    | Input voltage (under/overshoot)   | −0.5                                                             | V <sub>DDSHV</sub> + 0.5 | V    |
|                    | Clamp current for an input/output | −20                                                              | 20                       | mA   |
| T <sub>stg</sub>   | Storage temperature               | −65                                                              | 140                      | °C   |
|                    | ESD classification                | Class 2 (2.5 kV HBM, 500 V CDM, 150 V MM)                        |                          |      |
|                    | Moisture sensitivity              | Moisture sensitivity Class 3 (1 week floor life at 30°C / 60% H) |                          |      |

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

## RECOMMENDED OPERATING CONDITIONS

|                    |                                     |                                       | MIN  | TYP   | MAX  | UNIT |
|--------------------|-------------------------------------|---------------------------------------|------|-------|------|------|
| V <sub>DD</sub>    | Core supply voltage <sup>(1)</sup>  | 310 MHz, 5.7 A max. <sup>(2)(1)</sup> | 1.05 | 1.1   | 1.15 | V    |
|                    |                                     | {370 MHz} <sup>(3)</sup>              | 1.1  | 1.125 | 1.15 |      |
| V <sub>DDA</sub>   | Analog supply for PLLs              | 60 mA max. (each) <sup>(2)</sup>      | 1.71 | 1.8   | 1.89 |      |
| V <sub>DDS</sub>   | Digital supply voltage for LVDS I/O | 700 mA max. <sup>(2)</sup>            | 1.71 | 1.8   | 1.89 | V    |
| V <sub>DDSHV</sub> | Digital supply voltage CMOS I/O     | PC board design dependent             | 3.15 | 3.3   | 3.45 | V    |
| T <sub>C</sub>     | Case temperature                    |                                       | −40  | 30    | 90   | °C   |
| T <sub>J</sub>     | Junction temperature                | <sup>(4)</sup>                        |      |       | 105  | °C   |

- (1) Production tested hot using checksum at 310 MHz and maximum supplies. Power scales linearly with frequency with a dc consumption around 350 mA typical, 700 mA worst case.
- (2) Chip specifications are production tested to 90°C case temperature. QA tests are performed at 85°C.
- (3) Power consumption is a strong function of the configuration. A calculator is available to estimate power for a specific configuration.
- (4) Reliability calculations presume junction temperature 105°C or below. Operation above 105°C junction temperature reduces product lifetime.

## THERMAL INFORMATION

| THERMAL METRIC    |                                                             | GC5330   | UNIT |
|-------------------|-------------------------------------------------------------|----------|------|
|                   |                                                             | ZEV      |      |
|                   |                                                             | 484 PINS |      |
| $\theta_{JA}$     | Junction-to-ambient thermal resistance <sup>(1)</sup>       | 15.4     | °C/W |
| $\theta_{JCTop}$  | Junction-to-case (top) thermal resistance <sup>(2)</sup>    | 2.1      | °C/W |
| $\theta_{JB}$     | Junction-to-board thermal resistance <sup>(3)</sup>         | 7.6      | °C/W |
| $\psi_{JT}$       | Junction-to-top characterization parameter <sup>(4)</sup>   | 0.5      | °C/W |
| $\psi_{JB}$       | Junction-to-board characterization parameter <sup>(5)</sup> | 7.5      | °C/W |
| $\theta_{JCbott}$ | Junction-to-case (bottom) thermal resistance <sup>(6)</sup> | N/A      | °C/W |

- (1) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
- (2) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
- (3) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
- (4) The junction-to-top characterization parameter,  $\psi_{JT}$ , estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining  $\theta_{JA}$ , using a procedure described in JESD51-2a (sections 6 and 7).
- (5) The junction-to-board characterization parameter,  $\psi_{JB}$ , estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining  $\theta_{JA}$ , using a procedure described in JESD51-2a (sections 6 and 7).
- (6) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

## Pin Assignment and Descriptions (Top View)

|    | 1        | 2        | 3       | 4        | 5        | 6       | 7       | 8        | 9              | 10      | 11      | 12      | 13      | 14      | 15    | 16      | 17     | 18      | 19     | 20     | 21     | 22     |    |
|----|----------|----------|---------|----------|----------|---------|---------|----------|----------------|---------|---------|---------|---------|---------|-------|---------|--------|---------|--------|--------|--------|--------|----|
| A  | NC       | BBIN5P   | BBIN4P  | BBIN3P   | BBIN1P   | SPIDENB | SPICLK  | CEB      | UPA5           | UPA2    | UPD15   | UPD12   | UPD8    | UPD5    | UPD1  | VSSA2   | SYNCSB | SYNCSB  | SYNCSB | TXA1N  | TXA2P  | NC     | A  |
| B  | BBIN7N   | BBIN7P   | BBIN5N  | BBIN4N   | BBIN3N   | BBIN1N  | SPIDIO  | INTERRPT | UPA6           | UPA3    | WEB     | UPD13   | UPD9    | UPD6    | UPD2  | UPD0    | VDDA2  | SYNCSB  | TXA0N  | TXA1P  | TXA2N  | TXA5N  | B  |
| C  | BBIN8N   | BBIN8P   | BBIN6P  | BBIN6N   | VSSA1    | BBIN2P  | BBIN0P  | EMIFENA  | UPA7           | UPA4    | UPA0    | UPD14   | UPD10   | UPD7    | UPD3  | SYNCSB  | DPCLKP | TXA0P   | TXA3P  | TXA4P  | TXA4N  | TXA5P  | C  |
| D  | NC       | BBIN9N   | BBIN9P  | NC       | VDDA1    | BBIN2N  | BBIN0N  | VSS      | OEB            | VSS     | UPA1    | VSS     | UPD11   | VSS     | UPD4  | SYNCSB  | DPCLKN | TXA3N   | TXA6N  | TXA7N  | TXA8N  | TXA9P  | D  |
| E  | BBOUT0P  | BBIN10P  | BBIN10N | BBIN11P  | BBIN11N  | VDD     | VDD     | VDD      | VDD            | VDD     | VDD     | VDD     | VDD     | VDD     | VDD   | VDD     | NC     | NC      | TXA6P  | TXA7P  | TXA8P  | TXA9N  | E  |
| F  | BBOUT0N  | BBOUT2N  | BBOUT2P | BBOUT1N  | BBOUT1P  | NC      | VDDSHV2 | VDDSHV1  | VDD            | VDDSHV1 | VDD     | VDDSHV1 | VDD     | VDDSHV1 | VDD   | VDDSHV1 | NC     | VDD     | TXA11N | TXA11P | TXA10N | TXA10P | F  |
| G  | BBOUT4N  | BBOUT4P  | BBOUT3N | BBOUT3P  | VDDSHV2  | VSS     | VSS     | VSS      | VSS            | VSS     | VSS     | VSS     | VSS     | VSS     | VSS   | VSS     | VSS    | VDD     | TXA13P | TXA13N | TXA12P | TXA12N | G  |
| H  | BBOUT6N  | BBOUT6P  | BBOUT5N | BBOUT5P  | VDD      | VSS     | VSS     | VSS      | VSS            | VSS     | VSS     | VSS     | VSS     | VSS     | VSS   | VSS     | VSS    | VDDSHV1 | TXA15P | TXA15N | TXA14N | TXA14P | H  |
| J  | BBOUT8N  | BBOUT8P  | BBOUT7N | BBOUT7P  | VDD      | VSS     | VSS     | VSS      | VSS            | VSS     | VSS     | VSS     | VSS     | VSS     | VSS   | VSS     | VSS    | VDD     | TXA17P | TXA17N | TXA16N | TXA16P | J  |
| K  | BBOUT10N | BBOUT10P | BBOUT9N | BBOUT9P  | VDDSHV2  | VSS     | VSS     | VSS      | VSS            | VSS     | VSS     | VSS     | VSS     | VSS     | VSS   | VSS     | VSS    | VDDSHV1 | TXA19N | TXA19P | TXA18N | TXA18P | K  |
| L  | RXA13P   | RXA14N   | RXA14P  | BBOUT11P | BBOUT11N | VSS     | VSS     | VSS      | VSS            | VSS     | VSS     | VSS     | VSS     | VSS     | VSS   | VSS     | VSS    | VDD     | TXB1P  | TXB1N  | TXB0P  | TXB0N  | L  |
| M  | RXA13N   | RXA12P   | RXA11N  | RXA11P   | VDDSHV2  | VSS     | VSS     | VSS      | VSS            | VSS     | VSS     | VSS     | VSS     | VSS     | VSS   | VSS     | VSS    | VDDSHV1 | TXB3P  | TXB3N  | TXB2P  | TXB2N  | M  |
| N  | RXA12N   | RXA10P   | RXA9N   | RXA9P    | VDD      | VSS     | VSS     | VSS      | VSS            | VSS     | VSS     | VSS     | VSS     | VSS     | VSS   | VSS     | VSS    | VDD     | TXB5P  | TXB5N  | TXB4P  | TXB4N  | N  |
| P  | RXA10N   | RXA8N    | RXA8P   | RXA7N    | RXA7P    | VSS     | VSS     | VSS      | VSS            | VSS     | VSS     | VSS     | VSS     | VSS     | VSS   | VSS     | VSS    | VDD     | TXB7P  | TXB7N  | TXB6P  | TXB6N  | P  |
| R  | RXA6N    | RXA6P    | RXA5N   | RXA5P    | VDD      | VSS     | VSS     | VSS      | VSS            | VSS     | VSS     | VSS     | VSS     | VSS     | VSS   | VSS     | VSS    | VDDSHV1 | TXB9P  | TXB9N  | TXB8P  | TXB8N  | R  |
| T  | RXA4N    | RXA3N    | RXA3P   | RXA2N    | RXA2P    | VSS     | VSS     | VSS      | VSS            | VSS     | VSS     | VSS     | VSS     | VSS     | VSS   | VSS     | VSS    | VDD     | TXB11P | TXB11N | TXB10P | TXB10N | T  |
| U  | RXA4P    | RXA1P    | RXA0N   | RXA0P    | VDD      | NC      | VDDSHV2 | VDD      | VDDSHV2        | VDD     | VDDSHV2 | VDD     | VDDSHV2 | VDD     | VDD   | VDDSHV1 | NC     | VDD     | TXB13P | TXB13N | TXB12P | TXB12N | U  |
| V  | RXA1N    | RXB14N   | RXB10N  | RXB10P   | NC       | NC      | VDD     | VDD      | VDD            | VDD     | VDD     | VDD     | VDD     | VDD     | VDD   | VDD     | NC     | NC      | TXB15P | TXB15N | TXB14N | TXB14P | V  |
| W  | RXB14P   | RXB13P   | NC      | RXB6P    | RXB6N    | RXB4P   | RXB2P   | VPP      | VSS            | VPP     | VSS     | DVGA6   | VSS     | TDO     | TMS   | RXC6N   | RXC4N  | NC      | TXB17P | TXB17N | TXB16P | TXB16N | W  |
| Y  | RXB13N   | RXB12N   | RXB8N   | RXB8P    | RXB5P    | RXB4N   | RXB2N   | VDDMON   | RESETB         | DVGA13  | DVGA10  | DVGA7   | DVGA3   | DVGA0   | TDI   | RXC6P   | RXC5N  | RXC4P   | TXB19N | TXB19P | TXB18N | TXB18P | Y  |
| AA | RXB12P   | RXB11P   | RXB9P   | RXB7N    | RXB5N    | RXB3P   | RXB1N   | VSSMON   | SPIDIO (SPARE) | DVGA14  | DVGA11  | DVGA8   | DVGA4   | DVGA1   | TRSTB | RXC7N   | RXC5P  | RXC3P   | RXC2N  | RXC2P  | RXC0N  | NC     | AA |
| AB | NC       | RXB11N   | RXB9N   | RXB7P    | NC       | RXB3N   | RXB1P   | RXB0P    | RXB0N          | TESTMOD | DVGA15  | DVGA12  | DVGA9   | DVGA5   | DVGA2 | TCK     | RXC7P  | RXC3N   | RXC1N  | RXC1P  | RXC0P  | NC     | AB |



= 1.1 V



= 1.8 V, 3.3 V



= GND

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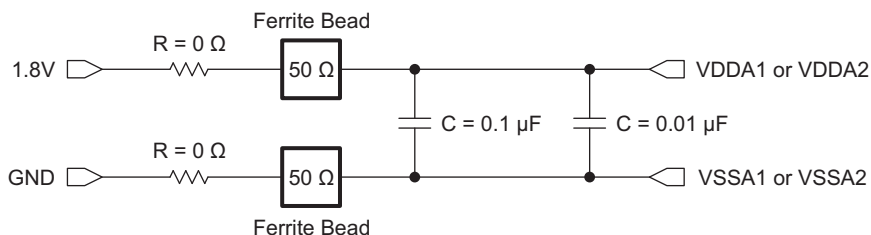
Figure 7. GC533x Pinout (Top View)

### Pin Functions

| NAME                           | NUMBER                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          | TYPE | DESCRIPTION                                   |
|--------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------|-----------------------------------------------|
| <b>POWER AND BIASING</b>       |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |      |                                               |
| VDD                            | E6, E7, E8, E9, E10, E11, E12, E13, E14, E15, E16, F9, F11, F13, F15, F18, G18, H5, J5, J18, L18, N5, N18, P18, R5, T18, U5, U8, U10, U12, U14, U15, U18, V7, V8, V9, V10, V11, V12, V13, V14, V15, V16                                                                                                                                                                                                                                                                                                                                                                                                         | PWR  | 1.1-V power supply                            |
| VDDSHV2                        | U9, U11, U13                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    | PWR  | 3.3-V power supply for CMOS I/O               |
| VDDSHV1                        | F8, F10, F12, F14                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               | PWR  | 3.3-V power supply for CMOS I/O               |
| VDDS1                          | F16, H18, K18, M18, R18, U16,                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   | PWR  | 1.8-V power supply for LVDS I/O               |
| VDDS2                          | F7, G5, K5, M5, U7                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              | PWR  | 1.8-V power supply for LVDS I/O               |
| VPP                            | W8, W10                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         | PWR  | 1.1-V E-fuse supply, connect to VDD           |
| VDDMON                         | Y8                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              | NC   | Do not connect, internal monitor point        |
| VSSMON                         | AA8                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             | NC   | Do not connect, internal monitor point        |
| VDDA2                          | B17                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             | PWR  | 1.8-V power for PLL (requires filtering)      |
| VDDA1                          | D5                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              | PWR  | 1.8-V power for PLL (requires filtering)      |
| VSSA2                          | A16                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             | PWR  | Ground for PLL (requires filtering)           |
| VSSA1                          | C5                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              | PWR  | Ground for PLL (requires filtering)           |
| VSS                            | D8, D10, D12, D14, G6, G7, G8, G9, G10, G11, G12, G13, G14, G15, G16, G17, H6, H7, H8, H9, H10, H11, H12, H13, H14, H15, H16, H17, J6, J7, J8, J9, J10, J11, J12, J13, J14, J15, J16, J17, K6, K7, K8, K9, K10, K11, K12, K13, K14, K15, K16, K17, L6, L7, L8, L9, L10, L11, L12, L13, L14, L15, L16, L17, M6, M7, M8, M9, M10, M11, M12, M13, M14, M15, M16, M17, N6, N7, N8, N9, N10, N11, N12, N13, N14, N15, N16, N17, P6, P7, P8, P9, P10, P11, P12, P13, P14, P15, P16, P17, R6, R7, R8, R9, R10, R11, R12, R13, R14, R15, R16, R17, T6, T7, T8, T9, T10, T11, T12, T13, T14, T15, T16, T17, W9, W11, W13 | PWR  | Ground                                        |
| NC                             | E17, E18, F6, F17, U6, U17, V5, V6, V17, V18                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    | NC   | No connection. Recommend connecting to ground |
| NC                             | A1, A22, D1, D4, W3, W18, AA22, AB1, AB5, AB22,                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 | NC   | No connection                                 |
| <b>BASEBAND INPUT/OUTPUT</b>   |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |      |                                               |
| BBIN[11:0]P                    | E4, E2, D3, C2, B2, C3, A2, A3, A4, C6, A5, C7                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  | I    | Baseband input – LVDS positive                |
| BBIN[11:0]N                    | E5, E3, D2, C1, B1, C4, B3, B4, B5, D6, B6, D7                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  | I    | Baseband input – LVDS negative                |
| BBOUT[11:0]P                   | L4, K2, K4, J2, J4, H2, H4, G2, G4, F3, F5, E1                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  | O    | Baseband output – LVDS positive               |
| BBOUT[11:0]N                   | L5, K1, K3, J1, J3, H1, H3, G1, G3, F2, F4, F1                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  | O    | Baseband output – LVDS negative               |
| <b>TX DAC INTERFACE</b>        |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |      |                                               |
| TXA[19:0]P                     | K20, K22, J19, J22, H19, H22, G19, G21, F20, F22, D22, E21, E20, E19, C22, C20, C19, A21, B20, C18                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              | O    | DAC TX port A – LVDS positive                 |
| TXA[19:0]N                     | K19, K21, J20, J21, H20, H21, G20, G22, F19, F21, E22, D21, D20, D19, B22, C21, D18, B21, A20, B19                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              | O    | DAC TX port A – LVDS negative                 |
| TXB[19:0]P                     | Y20, Y22, W19, W21, V19, V22, U19, U21, T19, T21, R19, R21, P19, P21, N19, N21, M19, M21, L19, L21                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              | O    | DAC TX port B – LVDS positive                 |
| TXB[19:0]N                     | Y19, Y21, W20, W22, V20, V21, U20, U22, T20, T22, R20, R22, P20, P22, N20, N22, M20, M22, L20, L22                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              | O    | DAC TX port B – LVDS negative                 |
| <b>RX and FB ADC INTERFACE</b> |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |      |                                               |
| RXA[14:0]P                     | L3, L1, M2, M4, N2, N4, P3, P5, R2, R4, U1, T3, T5, U2, U4                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      | I    | ADC receive port A – LVDS positive            |
| RXA[14:0]N                     | L2, M1, N1, M3, P1, N3, P2, P4, R1, R3, T1, T2, T4, V1, U3                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      | I    | ADC receive port A – LVDS negative            |
| RXB[14:0]P                     | W1, W2, AA1, AA2, V4, AA3, Y4, AB4, W4, Y5, W6, AA6, W7, AB7, AB8                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               | I    | ADC receive port B – LVDS positive            |
| RXB[14:0]N                     | V2, Y1, Y2, AB2, V3, AB3, Y3, AA4, W5, AA5, Y6, AB6, Y7, AA7, AB9                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               | I    | ADC receive port B – LVDS negative            |
| RXC[7:0]P                      | AB17, Y16, AA17, Y18, AA18, AA20, AB20, AB21                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    | I    | ADC receive port C – LVDS positive            |
| RXC[7:0]N                      | AA16, W16, Y17, W17, AB18, AA19, AB19, AA21                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     | I    | ADC receive port C – LVDS negative            |

## Pin Functions (continued)

| NAME                  | NUMBER                                                                                   | TYPE | DESCRIPTION                                                                                                                                                                                                                                   |
|-----------------------|------------------------------------------------------------------------------------------|------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <b>DVGA INTERFACE</b> |                                                                                          |      |                                                                                                                                                                                                                                               |
| DVGA[15:0]            | AB11, AA10, Y10, AB12, AA11, Y11, AB13, AA12, Y12, W12, AB14, AA13, Y13, AB15, AA14, Y14 | O    |                                                                                                                                                                                                                                               |
| <b>MPU INTERFACE</b>  |                                                                                          |      |                                                                                                                                                                                                                                               |
| UPD[15:0]             | A11, C12, B12, A12, D13, C13, B13, A13, C14, B14, A14, D15, C15, B15, A15, B16           | I/O  |                                                                                                                                                                                                                                               |
| UPA[7:0]              | C9, B9, A9, C10, B10, A10, D11, C11                                                      | I    |                                                                                                                                                                                                                                               |
| WEB                   | B11                                                                                      | I    | Write enable, active-low                                                                                                                                                                                                                      |
| EMIFENA               | C8                                                                                       | I    | EMIFENA switches between address/data $\mu$ P access and SPI access. Its value may be changed at any time, but both address/data access and SPI access must be idle during the change. Logic 1 = EMIF, logic 0 = SPI pin has internal pullup. |
| OEB                   | D9                                                                                       | I    | Read and output enable, active-low                                                                                                                                                                                                            |
| CEB                   | A8                                                                                       | I    | Chip enable, active-low                                                                                                                                                                                                                       |
| <b>JTAG INTERFACE</b> |                                                                                          |      |                                                                                                                                                                                                                                               |
| TRSTB                 | AA15                                                                                     | I    | JTAG reset (active-low); pull down if JTAG is not used.                                                                                                                                                                                       |
| TMS                   | W15                                                                                      | I    | JTAG mode select                                                                                                                                                                                                                              |
| TDO                   | W14                                                                                      | O    | JTAG data out                                                                                                                                                                                                                                 |
| TDI                   | Y15                                                                                      | I    | JTAG data in                                                                                                                                                                                                                                  |
| TCK                   | AB16                                                                                     | I    | JTAG clock                                                                                                                                                                                                                                    |
| <b>SPI INTERFACE</b>  |                                                                                          |      |                                                                                                                                                                                                                                               |
| SPIDENB               | A6                                                                                       | I    | Serial interface enable                                                                                                                                                                                                                       |
| SPICLK                | A7                                                                                       | I    | Serial interface clock                                                                                                                                                                                                                        |
| SPIDIO                | B7                                                                                       | I/O  | Serial interface data                                                                                                                                                                                                                         |
| SPIDO(SPARE)          | AA9                                                                                      | O    | Serial interface data out in four-wire SPI mode                                                                                                                                                                                               |
| <b>MISCELLANEOUS</b>  |                                                                                          |      |                                                                                                                                                                                                                                               |
| TESTMOD               | AB10                                                                                     | I    | Test mode for GC533x, typically grounded                                                                                                                                                                                                      |
| RESETB                | Y9                                                                                       | I    | Chip reset – required – active-low                                                                                                                                                                                                            |
| INTERRPT              | B8                                                                                       | O    | Output interrupt                                                                                                                                                                                                                              |
| DPDCLKP               | C17                                                                                      | I    | DPD CLK input – LVDS positive                                                                                                                                                                                                                 |
| DPDCLKN               | D17                                                                                      | I    | DPD CLK input – LVDS negative                                                                                                                                                                                                                 |
| SYNCOUTP              | A19                                                                                      | O    | Sync output – LVDS positive                                                                                                                                                                                                                   |
| SYNCOUTN              | A18                                                                                      | O    | Sync output – LVDS negative                                                                                                                                                                                                                   |
| SYNCAP                | C16                                                                                      | I    | Sync input A – LVDS positive                                                                                                                                                                                                                  |
| SYNCAN                | D16                                                                                      | I    | Sync input A – LVDS negative                                                                                                                                                                                                                  |
| SYNCBP                | B18                                                                                      | I    | Sync input B – LVDS positive                                                                                                                                                                                                                  |
| SYNCBN                | A17                                                                                      | I    | Sync input B – LVDS negative                                                                                                                                                                                                                  |



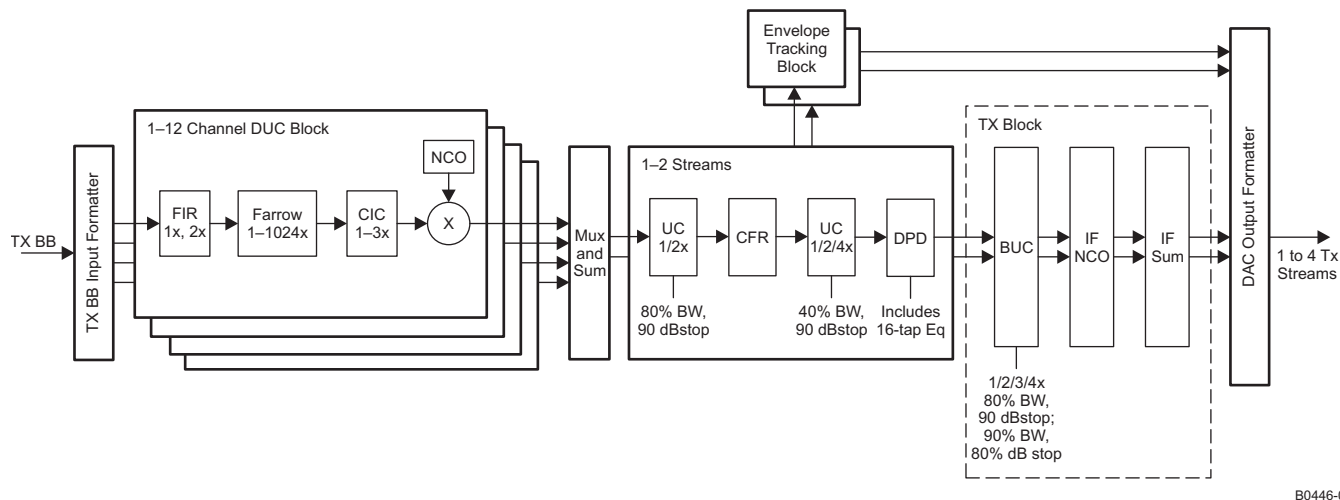
S0510-01

NOTE: 0- $\Omega$  R0603 resistor is used to accommodate series resistor if needed.**Figure 8. GC533x PLL Filtering**

The two GC533x PLLs require a filtered power supply. The supply can be generated by filtering the digital supply (VDDS1, VSSA1, VDDS2, and VSSA2). A representative filter is shown in Figure 8. The two PLLs should have separate filters that are located as close as is reasonable to their respective pins (especially the bypass capacitors). The ferrite beads should be series 50R (similar to Murata P/N: BLM31P500SPT, Description: IND FB BLM31P500SPT 50R 1206).

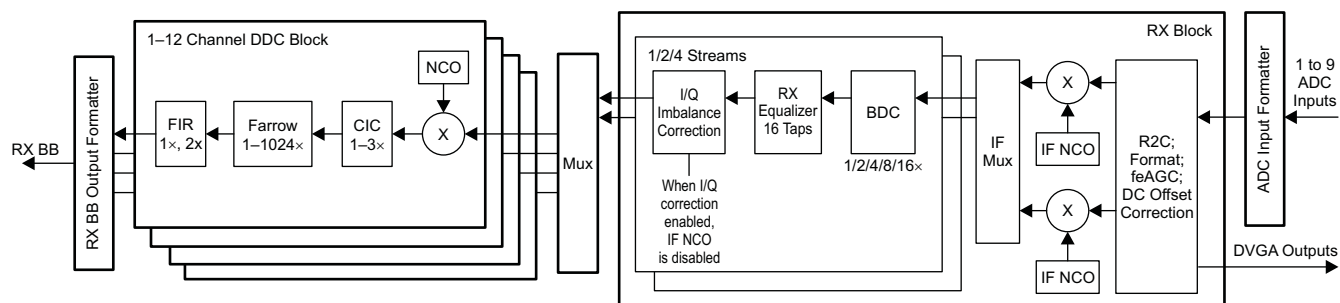
## Sub-Chip Descriptions

Figure 9 shows the TX functional block diagram, and Figure 10 shows the RX functional block diagram. Note that each figure shows up to four DUC or DDC blocks in the TX or RX paths, and there are a total of four DDUC blocks that may be configured as either DUC or DDC each.



B0446-01

Figure 9. TX Functional Block Diagram



B0447-01

Figure 10. RX Functional Block Diagram

## TX Baseband Input Formatter

The TX baseband (BB) input-formatter block accepts TX baseband inputs from the FPGA or baseband processor and formats them for the DUC blocks. There are 12 unidirectional LVDS pairs for the TX input formatter, and their function depends on the operational mode. There are three operational modes for the TX BB input formatter: byte mode (B, 8 or 9 bits), nibble mode (N, 4 bits), and serial mode (S, 2 bits) to allow multiple BB input rates. The GC533x can accept up to three different BB input data rates. Table 2 and Table 3 summarize each mode and the pin assignments. In Table 3, BBIN[X] is the BBIN differential pair (assumed positive and negative connections), and BB0, BB1, and BB2 represent three different TX baseband ports at arbitrary rates.

**Table 2. TX BB Formatter Modes**

| MODE              | DESCRIPTION                                                                       | Total Number of Interface Pins                                                   | Maximum Complex Interface Rate per Channel<br>N is the number of channels.                                                                |
|-------------------|-----------------------------------------------------------------------------------|----------------------------------------------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------|
| 1B                | Byte mode, 1 interface rate                                                       | 10 or 11 = 8 or 9 data + 1 clk + 1 sync                                          | $(\text{Clk} \times 4/4)/N$ ; maximum 192.31 MSPS total (for all channels)                                                                |
| 1N                | Nibble mode, 1 interface rate                                                     | 6 = 4 data + 1 clk + 1 sync                                                      | $(\text{Clk} \times 4/8)/N$ ; maximum 125 (Nibble 0), 96.15 (Nibble 1) MSPS total                                                         |
| 1S                | Serial mode, 1 interface rate                                                     | 4 = 2 data + 1 clk + 1 sync                                                      | $(\text{Clk} \times 4/16)/N$ ; maximum 48.07 MSPS total                                                                                   |
| 2N                | Nibble mode, 2 interface rates                                                    | 12 = 4 data + 1 clk + 1 sync + 4 data + 1 clk + 1 sync                           | $(\text{Clk} \times 4/8)/N \times 2$ ; maximum 221.15 MSPS total                                                                          |
| 2N <sup>(1)</sup> | Nibble + byte mode, 2 interface rates, RX-ADC input pins used for byte-mode port. | 16 = 4 data + 1 clk + 1 sync + 8 data + 1 clk + 1 sync                           | Nibble port: $(\text{Clk} \times 4/8)/N$ ; maximum 125 MSPS total<br>Byte port: $(\text{Clk} \times 2/4)/N$ ; maximum 125, 250 MSPS total |
| 2S                | Serial mode, 2 interface rates                                                    | 8 = 2 data + 1 clk + 1 sync + 2 data + 1 clk + 1 sync                            | $(\text{Clk} \times 4/16)/N$ ; maximum 96.15 MSPS total                                                                                   |
| 3S                | Serial mode, 3 interface rates                                                    | 12 = 2 data + 1 clk + 1 sync + 2 data + 1 clk + 1 sync + 2 data + 1 clk + 1 sync | $(\text{Clk} \times 4/16)/N$ ; maximum 144.23 MSPS total                                                                                  |

(1) 2N' is the only configuration that allows a special mode to re-use RX input port A as baseband TX inputs

**Table 3. TX BB Pin Assignments**

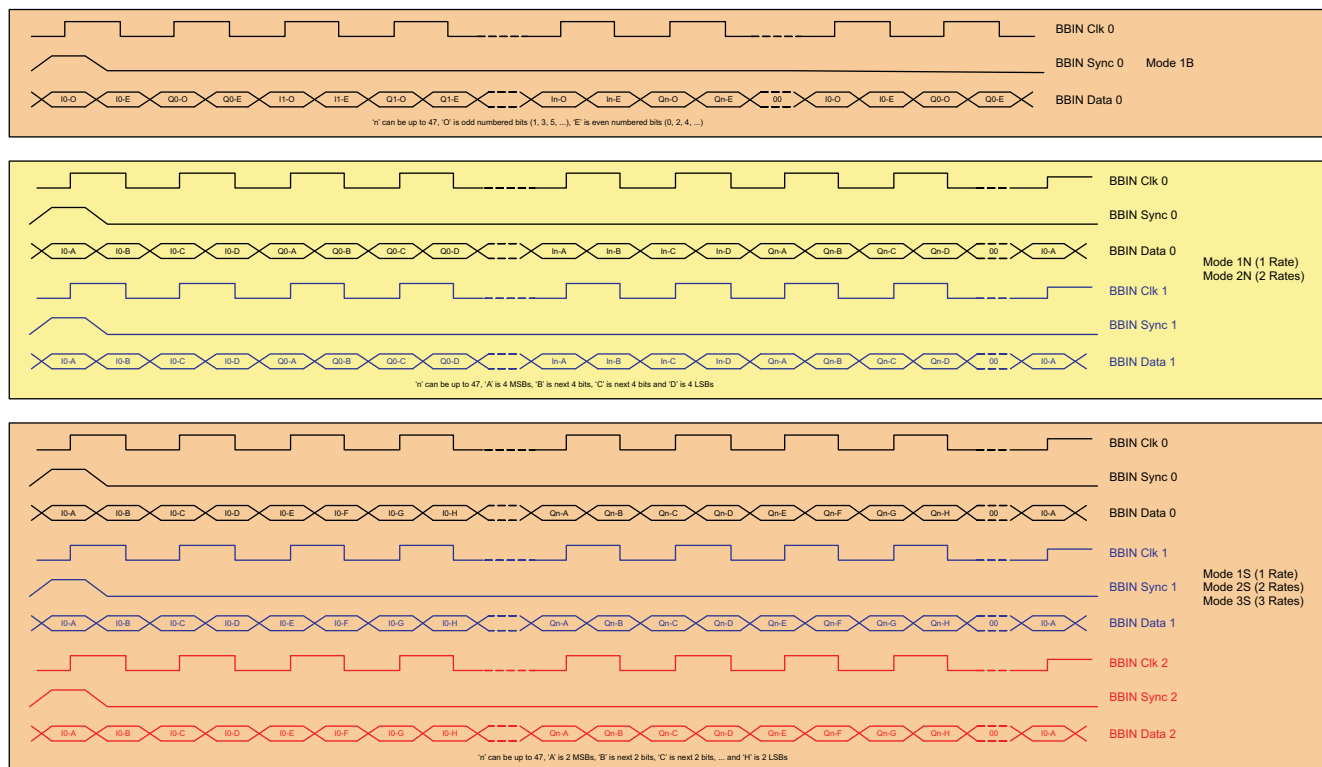
| LVDS PAIR BBI[11:0]                               | BYTE MODE  | NIBBLE MODE | SERIAL MODE |
|---------------------------------------------------|------------|-------------|-------------|
| BBIN[0] pos. and neg.                             | BB0_DATA_0 | BB0_DATA_0  | BB0_DATA_0  |
| BBIN[1] pos. and neg.                             | BB0_DATA_1 | BB0_DATA_1  | BB0_DATA_1  |
| BBIN[2] pos. and neg.                             | BB0_DATA_2 | BB0_SYNC    | BB0_SYNC    |
| BBIN[3] pos. and neg.                             | Spare      | BB0_CLOCK   | BB0_CLOCK   |
| BBIN[4] pos. and neg.                             | BB0_DATA_3 | BB0_DATA_2  | BB1_DATA_0  |
| BBIN[5] pos. and neg.                             | BB0_DATA_4 | BB0_DATA_3  | BB1_DATA_1  |
| BBIN[6] pos. and neg.                             | BB0_SYNC   | BB1_SYNC    | BB1_SYNC    |
| BBIN[7] pos. and neg.                             | BB0_CLOCK  | BB1_CLOCK   | BB1_CLOCK   |
| BBIN[8] pos. and neg.                             | BB0_DATA_5 | BB1_DATA_0  | BB2_DATA_0  |
| BBIN[9] pos. and neg.                             | BB0_DATA_6 | BB1_DATA_1  | BB2_DATA_1  |
| BBIN[10] pos. and neg.                            | BB0_DATA_7 | BB1_DATA_2  | BB2_SYNC    |
| BBIN[11] pos. and neg.                            | BB0_DATA_8 | BB1_DATA_3  | BB2_CLOCK   |
| Number of BBdata streams                          | 1          | 2           | 3           |
| Number of DDR clocks to transfer 1 complex sample | 2          | 4           | 8           |

The actual data transfer rate in nibble mode is 2 times higher than the byte mode for the same total throughput. If two ports are required (e.g., to support two different sample rates), and a lower speed on the interface is desired, the GC533x can re-use the RX ADC input port A as a baseband TX input bus. RX ADC port A has 15 pairs of LVDS input pins and supports one set of baseband input data in byte mode. When RX port A is used as a baseband TX input, it cannot be also used as an RX input port.

The baseband interface supports a full-clock or gated-clock format. These formats are shown in [Figure 11](#)

The mapping for the RX port A pins when in BB TX input mode is:

- RXA14: clock
- RXA13: sync
- RXA12–5: BB0\_DATA7–0



T0504-01

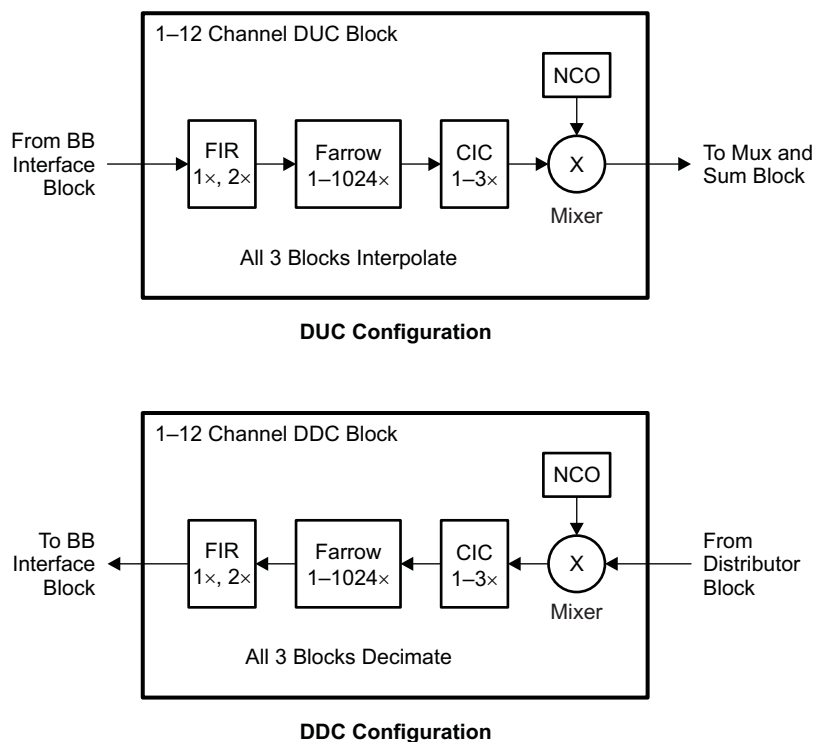
### Figure 11. TX BB Formats

The TX formatter block includes a per-channel TX gain adjust via a 16-bit complex digital word which can be set to have gain between  $-\infty$  and 9 dB.

## Digital Down- and Upconverters (DDUCs)

The GC533x has four identical and independent DDUC blocks that can be configured as either DDC or DUC. Each DDUC can support up to 12 channels with scalable bandwidth.

The only difference between the DUC and DDC configurations is the interpolate (DUC) versus decimate (DDC) functions and the data path direction as shown in [Figure 12](#). Both DDC and DUC are described in this section. Note that each DDUC block must be configured statically as a DUC or DDC and cannot switch modes dynamically in TDD applications.



B0448-01

**Figure 12. DUC and DDC Functional Block Diagram**

In combination with the follow-on mux and sum block, the DUC block interpolates, filters, mixes each carrier, and combines multiple channels into one to four wideband, composite TX signal streams. Any input channel can be mapped to any TX stream in the mux and sum block.

The DDC configuration accepts an RX stream from the distributor block and provides mixing, decimation filtering, fractional resampling, and filtering to RX channels. The RX block outputs are mapped to the mixer CIC stream via the distributor block.

Each DDUC block contains a finite impulse response (FIR) filter, a fractional resampler (Farrow filter), a cascaded integrator-comb (CIC) filter, a complex mixer and NCO for channel placement in the composite stream, and a programmable frequency hopper (see [Figure 12](#)).

The number of taps available in the FIR filter depends on various parameters such as the BBclk rate (derived from DPDCLK), input sample rate, interpolate and decimate settings, and number of channels. Different tap values may be used for each channel (however, that reduces the number of filter taps available).

Note that the input sample rate is the input from the TX BB input formatter for the DUC configuration and the input from the distributor block for DDC configuration. The number of taps for various wireless standards and configurations is shown in [Table 4](#).

The Farrow filter supports one real channel or 1–12 complex channels and can be configured for any resampling ratio from 1 to 1024 with 32-bit resolution. A different delay value for each channel is supported. The Farrow filter is used to resample different TX BB input sample rates to a common CFR and DPD sample rate, and it provides 95-dB rejection at  $\pm 0.25$  output  $f_s$  (sample rate), 83-dB rejection at  $\pm 0.375$  output  $f_s$ , and 56-dB rejection at  $\pm 0.4$  output  $f_s$ .

The CIC interpolates or decimates by a factor of 1, 2, or 3. If each DDUC must support more than eight carriers, the CIC must interpolate/decimate by 3. If each DDUC must support between four and eight carriers, the CIC can interpolate/decimate by 2 or 3. If each DDUC must support fewer than four carriers, the CIC can interpolate by 1, 2, or 3.

The NCO contains a 48-bit frequency word and 48-bit accumulator, and operates at the DUC output sample rate. The minimum resolution is the DUC output sample rate or DDC input sample rate divided by  $2^{48}$ , or about 0.2  $\mu$ Hz for a 61.44-MSPS DUC output rate. The mixer and NCO can be used for frequency planning or fine frequency control.

Per-channel phase can be adjusted in the mixer/NCO block with a 16-bit phase word, while per channel fractional delay can be adjusted in the Farrow block.

**Table 4. Number of FIR Filter Taps for Example Signal Types**

| Name             | BBclk  | Input Sample Rate | Filter Type   | DUC Mode Interp. | DDC Mode Decim. | No. of Channels | Max. Taps |
|------------------|--------|-------------------|---------------|------------------|-----------------|-----------------|-----------|
|                  | MHz    | MSPS              | Sym or Un-Sym | 1 or 2           | 1 or 2          |                 |           |
| lte20_1          | 245.76 | 30.72             | S             | 1                | 1               | 1               | 159       |
| lte20_2          | 245.76 | 30.72             | S             | 1                | 1               | 2               | 79        |
| lte10_2          | 245.76 | 15.36             | S             | 1                | 1               | 2               | 159       |
| lte10_3          | 245.76 | 15.36             | S             | 1                | 1               | 3               | 99        |
| lte10_4          | 245.76 | 15.36             | S             | 1                | 1               | 4               | 79        |
| lte5_4           | 245.76 | 7.68              | S             | 1                | 1               | 4               | 159       |
| lte5_8           | 245.76 | 7.68              | S             | 1                | 1               | 8               | 79        |
| wimax20_r3       | 246.4  | 44.8              | S             | 1                | 2               | 3               | 59        |
| wimax20_t3       | 246.4  | 22.4              | S             | 2                | 1               | 3               | 39        |
| wimax20_r2       | 246.4  | 44.8              | S             | 1                | 2               | 2               | 99        |
| wimax20_t2       | 246.4  | 22.4              | S             | 2                | 1               | 2               | 79        |
| wimax20_r1       | 246.4  | 44.8              | S             | 1                | 2               | 1               | 219       |
| wimax20_t1       | 246.4  | 22.4              | S             | 2                | 1               | 1               | 199       |
| wimax10_r2       | 246.4  | 22.4              | S             | 1                | 2               | 2               | 219       |
| wimax10_t2       | 246.4  | 11.2              | S             | 2                | 1               | 2               | 199       |
| wimax10_r3       | 246.4  | 22.4              | S             | 1                | 2               | 3               | 139       |
| wimax10_t3       | 246.4  | 11.2              | S             | 2                | 1               | 3               | 119       |
| wimax10_r4       | 246.4  | 22.4              | S             | 1                | 2               | 4               | 99        |
| wimax10_t4       | 246.4  | 11.2              | S             | 2                | 1               | 4               | 79        |
| wimax5_r4        | 246.4  | 11.2              | S             | 1                | 2               | 4               | 219       |
| wimax5_t4        | 246.4  | 5.6               | S             | 2                | 1               | 4               | 199       |
| wimax5_r8        | 246.4  | 11.2              | S             | 1                | 2               | 8               | 99        |
| wimax5_t8        | 246.4  | 5.6               | S             | 2                | 1               | 8               | 79        |
| wbcdma_r4        | 245.76 | 7.68              | S             | 1                | 1               | 4               | 159       |
| wbcdma_t4        | 245.76 | 3.84              | S             | 2                | 1               | 4               | 319       |
| wbcdma_r8        | 245.76 | 7.68              | S             | 1                | 1               | 8               | 79        |
| wbcdma_t8        | 245.76 | 3.84              | S             | 2                | 1               | 8               | 159       |
| cdma_r12         | 245.76 | 2.4576            | S             | 1                | 1               | 12              | 99        |
| cdma_t12         | 245.76 | 1.2288            | U             | 2                | 1               | 12              | 100       |
| tdscdma_r12      | 245.76 | 2.56              | S             | 1                | 1               | 12              | 99        |
| tdscdma_t12      | 245.76 | 1.28              | S             | 2                | 1               | 12              | 199       |
| gsm_12           | 243.8  | 0.5417            | S             | 1                | 1               | 12              | 99        |
| eedge_12         | 243.8  | 1.625             | S             | 1                | 1               | 12              | 99        |
| wideband_60MHz_r | 250    | 75                | S             | 1                | 1               | 1               | 59        |
| wideband_60MHz_t | 250    | 75                | S             | 2                | 1               | 1               | 39        |

## MUX and SUM (TX Direction)

The MUX and SUM block maps any channel from the DUC to any TX stream for subsequent per-stream processing.

## Crest Factor Reduction (CFR)

The CFR blocks include the CFR function and two interpolate-by-2 filters (referred to here as UC1 and UC2). The two CFR blocks together can support 1, 2, or 4 TX streams. The CFR function selectively reduces the peak-to-average ratio (PAR) of wideband digital signals provided in quadrature (I and Q) format, such as those used in 3G and 4G wireless applications. For example, the CFR function can reduce the PAR of WCDMA Test Model 1 signals to 5.7 dB, while still meeting all 3GPP requirements for ACLR, composite EVM, and peak code domain error (PCDE).

The CFR blocks can be configured in eleven different modes, depending on the number of TX streams, the DPD mode, and the signal sample rates. Relative to previous TI CFR products, the GC533x CFR has enhanced features such as:

- Constant PAR mode
- Constant input-to-output power mode
- Dynamic PAR target levels for different portions of the time-domain signal
- Up to 25% less latency for certain configurations
- Enhanced CFR performance for narrowband signals
- Automatic (i.e., no host interaction required) CFR coefficient generation for frequency-hopping signals

The UC1 and UC2 blocks can be set to 1× or 2× interpolation and may be used to provide optimum selection of signal oversampling ratio at CFR. UC1 may be positioned before or after the CFR function, while UC2 is always at the output of CFR. Since UC2 has only a 40% bandwidth image rejection (90 dB) filter, it is only used if preceded by UC1, which has an 80% bandwidth image-rejection (90 dB) filter.

## Digital Predistortion (DPD)

The DPD blocks include the DPD function, TX equalization, and the envelope tracking (ET) function. The GC533x supports two modes of operation, depending on signal bandwidth and desired DPD correction capability: high-performance (HP) mode and high-bandwidth (HB) mode. For 5× DPD expansion bandwidth (fifth-order DPD correction), the following signal bandwidths and number of streams can be supported.

### High-performance DPD mode

- 1 TX stream at 62 {74} MHz
- 2 TX streams at 31 {37} MHz each
- 4 TX streams at 15.5 {18.5} MHz each

This mode provides more extensive nonlinear correction or longer DPD memory and is suitable for the most-difficult and high-performance DPD requirements.

### High-bandwidth DPD mode

- 1 TX stream at 62 {74} MHz
- 2 TX streams at 62 {74} MHz each
- 4 TX streams at 31 {37} MHz each

This mode provides excellent DPD correction for most DPD requirements.

The TX equalizer is a complex equalizer and is configurable from 17 to 34 taps, depending on the DPD mode of operation. In HP modes, the number of taps may be up to 34. In HB modes, the number of taps may be up to 17. Contact the TI factory for additional details.

The predistortion correction terms are computed by an external processor (e.g., TI TMS320C6748 DSP) based on reference-input and PA-feedback data captured in the GC533x capture buffers. The external processor reads the captured data buffers from the GC533x and writes back the newly computed DPD correction terms on a continuous basis.

## DPD – Envelope Tracking (ET) Mode

The ET block provides a 10-, 12-, or 14-bit real digital word, at a rate up to 155 MSPS, that is proportional to the peak envelope signal of the composite TX stream either before or after the DPD function. The ET block includes fixed and fractional delay adjustments and a LUT to provide nonlinear shaping to the ET waveform. The GC533x can provide one or two ET outputs along with the corresponding one or two TX signal stream outputs. The ET outputs use one of the LVDS DAC ports and have two interface format modes:

- a. One or two antenna streams. One antenna stream per port, with interleaved MSB half-word and LSB half-word. The port can be configured as 7-, 6-, or 5-bit DDR data (see [Table 14](#) and [Figure 18](#)), plus clock (maximum clock rate of 155 MHz in this mode). In all three cases, the 16-bit internal data is rounded to the specified 14, 12, or 10 bits. Format on the DDR data port for the three cases is:
  - 14-bit: [13:7], then [6:0]
  - 12-bit: [11:6], then [5:0]
  - 10-bit: [9:5], then [4:0]
- b. One antenna stream only. One antenna stream per port. The port can be configured as 14-, 12-, or 10-bit SDR data (see [Figure 18](#)), plus clock (maximum clock rate of 155 MHz in this mode). In all three cases, the 16-bit internal data is rounded to the specified 14, 12, or 10 bits.

Note that clock out may have a few hundred ps of jitter and is not suitable for directly driving the ET modulator DAC. The clock for the ET modulator DAC should come directly from a TI CDC clock chip, which is already on the board to provide clock sources.

## TX IF Sub-Chip

The TX IF sub-chip includes a bulk upconverter (BUC), four IF mixer/NCO blocks, and TX stream MUX and SUM.

The BUC block has interpolations of 1×, 1.5×, 2×, 3×, and 4×. In the DPD high-band width mode, the 2× interpolation from the BUC is routed to the DPD input. In the high-bandwidth mode, BUC interpolation is not used after DPD. In the DPD high-performance mode, BUC interpolation is dependent on the configuration.

There are four parallel NCO/MIX blocks to allow frequency translation of each composite TX stream. The NCO is 48 bits and is referenced to the TX output rate. The NCO/MIX block can be used in either HP or HB modes; however, using the mixer reduces the DPD expansion bandwidth by the amount of frequency translation.

The TX stream MUX and SUM block allows summing of TX streams to create composite TX streams.

## TX DAC Formatter

The DAC output consists of two 20-pair LVDS blocks that can be configured by the DAC formatter block for several TI DACs and system configurations. The formatter can support up to 8 DACs for 4 TX streams in complex mode. The DAC formatter block supports the TI DAC5682, DAC328x, and DAC348x families. [Table 5](#) illustrates the pin connections the different DAC and envelope [ET] modulator types.

Table 5. GC533x DAC Interface Pin Map

| GC533x | 328x (ET)  | 3482 Byte  | 5682       | 3484       | 3482 Word  |
|--------|------------|------------|------------|------------|------------|
| TXA0   | P1-d7      | P1-d7      | P1-sync    | P1-sync    | P1-sync    |
| TXA1   | P1-d6      | P1-d6      | P1-d15     | P1-d15     | P1-d15     |
| TXA2   | P1-d5      | P1-d5      | P1-d14     | P1-d14     | P1-d14     |
| TXA3   | P1-d4      | P1-d4      | P1-d13     | P1-d13     | P1-d13     |
| TXA4   | P1-dataclk | P1-dataclk | P1-d12     | P1-d12     | P1-d12     |
| TXA5   | P1-frame   | P1-frame   | P1-d11     | P1-d11     | P1-d11     |
| TXA6   | P1-d3      | P1-d3      | P1-d10     | P1-d10     | P1-d10     |
| TXA7   | P1-d2      | P1-d2      | P1-d9      | P1-d9      | P1-d9      |
| TXA8   | P1-d1      | P1-d1      | P1-d8      | P1-d8      | P1-d8      |
| TXA9   | P1-d0      | P1-d0      | P1-dataclk | P1-dataclk | P1-dataclk |
| TXA10  | P2-d7      | P2-d7      | NA         | P1-frame   | NA         |
| TXA11  | P2-d6      | P2-d6      | P1-d7      | P1-d7      | P1-d7      |
| TXA12  | P2-d5      | P2-d5      | P1-d6      | P1-d6      | P1-d6      |
| TXA13  | P2-d4      | P2-d4      | P1-d5      | P1-d5      | P1-d5      |
| TXA14  | P2-dataclk | P2-dataclk | P1-d4      | P1-d4      | P1-d4      |
| TXA15  | P2-frame   | P2-frame   | P1-d3      | P1-d3      | P1-d3      |
| TXA16  | P2-d3      | P2-d3      | P1-d2      | P1-d2      | P1-d2      |
| TXA17  | P2-d2      | P2-d2      | P1-d1      | P1-d1      | P1-d1      |
| TXA18  | P2-d1      | P2-d1      | P1-d0      | P1-d0      | P1-d0      |
| TXA19  | P2-d0      | P2-d0      | NA         | P1-parity  | P1-parity  |
| TXB0   | P3-d7      | P3-d7      | P2- sync   | P2-sync    | P2-sync    |
| TXB1   | P3-d6      | P3-d6      | P2-d15     | P2-d15     | P2-d15     |
| TXB2   | P3-d5      | P3-d5      | P2-d14     | P2-d14     | P2-d14     |
| TXB3   | P3-d4      | P3-d4      | P2-d13     | P2-d13     | P2-d13     |
| TXB4   | P3-dataclk | P3-dataclk | P2-d12     | P2-d12     | P2-d12     |
| TXB5   | P3-frame   | P3-frame   | P2-d11     | P2-d11     | P2-d11     |
| TXB6   | P3-d3      | P3-d3      | P2-d10     | P2-d10     | P2-d10     |
| TXB7   | P3-d2      | P3-d2      | P2-d9      | P2-d9      | P2-d9      |
| TXB8   | P3-d1      | P3-d1      | P2-d8      | P2-d8      | P2-d8      |
| TXB9   | P3-d0      | P3-d0      | P2-dataclk | P2-dataclk | P2-dataclk |
| TXB10  | P4-d7      | P4-d7      | NA         | P2-frame   | NA         |
| TXB11  | P4-d6      | P4-d6      | P2-d7      | P2-d7      | P2-d7      |
| TXB12  | P4-d5      | P4-d5      | P2-d6      | P2-d6      | P2-d6      |
| TXB13  | P4-d4      | P4-d4      | P2-d5      | P2-d5      | P2-d5      |
| TXB14  | P4-dataclk | P4-dataclk | P2-d4      | P2-d4      | P2-d4      |
| TXB15  | P4-frame   | P4-frame   | P2-d3      | P2-d3      | P2-d3      |
| TXB16  | P4-d3      | P4-d3      | P2-d2      | P2-d2      | P2-d2      |
| TXB17  | P4-d2      | P4-d2      | P2-d1      | P2-d1      | P2-d1      |
| TXB18  | P4-d1      | P4-d1      | P2-d0      | P2-d0      | P2-d0      |
| TXB19  | P4-d0      | P4-d0      | NA         | P2-parity  | P2-parity  |

Note: P1, P2, P3, and P4 are used to identify a specific DAC port. Different ports have different timing.

## RX ADC Formatter

There are three ADC input ports: two 15-pair LVDS ports (referred to as ports A and B) and one 8-pair LVDS port (referred to as port C and typically used for the DPD feedback path). Depending on the ADCs selected, these three ports can accommodate up to 17 ADCs (e.g., using two octals and a single). The formatter block can route any port to either the capture buffer block or the RX signal processing blocks. The pin connections for the ADCs are shown in [Table 6](#).

The GC533x works seamlessly with the following TI ADCs.

**Single:** 5400, 12-bit, 1 GSPS, may need special routing on the PCB.

5463, 12-bit, 500 MSPS, may need clock-to-data-skew special routing on the PCB.

54RF63, 12-bit, 550 MSPS, may need clock-to-data-skew special routing on the PCB.

5474, 14-bit, 400 MSPS, may need clock-to-data-skew special routing on the PCB.

5493, 16-bit, 130 MSPS

548x, 16-bit, 80-200 MSPS

612x, 12-bit, 65–250 MSPS

614x, 14-bit, 65-250 MSPS

58B18, 11-bit, 200 MSPS

414x, 14-bit, 160–250 MSPS

412x, 12-bit, 160–250 MSPS

552x, 12-bit, 170–210 MSPS

554x, 14-bit, 170–210 MSPS

5517, 11-bit, 200 MSPS

### Dual:

62c15, 11-bit, 125 MSPS

62c17, 11-bit, 200 MSPS

58c28, 11-bit, 200 MSPS

62p4x, 14-bit, 65-250 MSPS

62p2x, 12-bit, 65-250 MSPS

624x, 14-bit, 65-125 MSPS

622x, 12-bit, 65-125 MSPS

### Quad:

642x, 12-bit, 65–125 MSPS

644x, 14-bit, 65–125 MSPS

### Octal:

527x, 12-bit, 65 MSPS

528x, 12-bit, 65 MSPS

Table 6. GC533x ADC Interface Pin Map

| GC533x<br>Pin Name | 58b18 5517<br>4149 61B49<br>5547 | 548x 6145 | 58c48 42x9<br>64p4x<br>62p4x<br>62c15 | 5463 5444<br>5474 | 5400L               | 5400R   | 642x 644x | 527x 528x | Two 624x |
|--------------------|----------------------------------|-----------|---------------------------------------|-------------------|---------------------|---------|-----------|-----------|----------|
| RXA0               | 0                                |           | 0                                     | 0                 | [12] <sup>(1)</sup> | syncout | [istrobe] |           |          |
| RXA1               | 2                                |           | 2                                     | 1                 | 11                  | 0       |           |           |          |
| RXA2               | 4                                |           | 4                                     | 2                 | 10                  | 1       | d1        |           | b1       |
| RXA3               | 6                                | 0         | 6                                     | 3                 | 9                   | 2       | d0        |           | b0       |
| RXA4               | 8                                | 2         | 8                                     | 4                 | 8                   | 3       | c1        |           | f        |
| RXA5               | 10                               | 4         | 10                                    | 5                 | 7                   | 4       | c0        | c0        | a1       |
| RXA6               | 12                               | 6         | 12                                    | 6                 | 6                   | 5       | frame     | c1        | a0       |
| RXA7               | clk                              | clk       | clk                                   | 7                 | clk                 | clk     | clk       | clk       | clk      |
| RXA8               | [14]                             | 8         | 0                                     | 8                 | 5                   | 6       | b1        | c2        |          |
| RXA9               |                                  | 10        | 2                                     | 9                 | 4                   | 7       | b0        | c3        | b1       |
| RXA10              |                                  | 12        | 4                                     | 10                | 3                   | 8       | a1        | c4        | b0       |
| RXA11              |                                  | 14        | 6                                     | 11                | 2                   | 9       | a0        | c5        | f        |
| RXA12              |                                  |           | 8                                     | 12                | 1                   | 10      |           | c6        | a1       |
| RXA13              |                                  |           | 10                                    | 13                | 0                   | 11      |           | c7        | a0       |
| RXA14              | [istrobe]                        | [istrobe] | 12                                    | clk               | syncout             | [12]    |           | fr        | clk      |
| RXB0               | 0                                |           | 0                                     | 0                 | [12]                | syncout |           |           |          |
| RXB1               | 2                                |           | 2                                     | 1                 | 11                  | 0       |           |           |          |
| RXB2               | 4                                |           | 4                                     | 2                 | 10                  | 1       |           |           |          |
| RXB3               | 6                                | 0         | 6                                     | 3                 | 9                   | 2       |           |           |          |
| RXB4               | 8                                | 2         | 8                                     | 4                 | 8                   | 3       |           |           |          |
| RXB5               | 10                               | 4         | 10                                    | 5                 | 7                   | 4       |           |           |          |
| RXB6               | 12                               | 6         | 12                                    | 6                 | 6                   | 5       |           |           |          |
| RXB7               | clk                              | clk       | clk                                   | 7                 | clk                 | clk     |           |           |          |
| RXB8               | [14]                             | 8         | 0                                     | 8                 | 5                   | 6       |           |           |          |
| RXB9               |                                  | 10        | 2                                     | 9                 | 4                   | 7       |           |           |          |
| RXB10              |                                  | 12        | 4                                     | 10                | 3                   | 8       |           |           |          |
| RXB11              |                                  | 14        | 6                                     | 11                | 2                   | 9       |           |           |          |
| RXB12              |                                  |           | 8                                     | 12                | 1                   | 10      |           |           |          |
| RXB13              |                                  |           | 10                                    | 13                | 0                   | 11      |           |           |          |
| RXB14              | [istrobe]                        | [istrobe] | 12                                    | clk               | syncout             | [12]    |           |           |          |
| RXC0               | 0                                |           |                                       |                   |                     |         |           |           |          |
| RXC1               | 2                                |           |                                       |                   |                     |         |           |           |          |
| RXC2               | 4                                |           |                                       |                   |                     |         |           |           |          |
| RXC3               | 6                                |           |                                       |                   |                     |         |           |           |          |
| RXC4               | 8                                |           |                                       |                   |                     |         |           |           |          |
| RXC5               | 10                               |           |                                       |                   |                     |         |           |           |          |
| RXC6               | 12                               |           |                                       |                   |                     |         |           |           |          |
| RXC7               | clk                              |           |                                       |                   |                     |         |           |           |          |

(1) [ ] indicates assignment if pins available

## Feedback Processing

The feedback path is input to RXC as a real ADC. This is captured in the capture buffer and sent to the DSP. In cases where a higher-rate real ADC (>250 Msps) or a complex feedback path is desired, for better feedback performance, one of the RX ADC inputs can be used for the feedback path, and one RX ADC input is used for the RX path. Note: both RX downconverters can still be used for the RX path, or one can be used for feedback.

The widest-band feedback is seen directly from the ADC interface to the capture buffer. Further RX processing to get the complex data to the capture buffer requires that the complex rate is one-half the DPD clock rate or lower.

## RX Sub-Chips

Each of two RX sub-chips consists of the following blocks (each block may be optionally bypassed), which operate on a per-stream basis:

- DC offset cancellation
- Front-end automatic gain control (feAGC)
- Real-to-Complex (R2C) conversion
- Switch for replicating or moving streams across the four paths (per sub-chip)
- IF NCO for complex mixing (frequency translation)
- Bulk downconverter (BDC)
- Equalizer
- IQ imbalance correction

### DC offset cancellation

The dc offset canceller can be programmed to integrate a number of input samples automatically, divide by a power of 2, and subtract the mean offset or a programmed offset from the input. The input can be real or complex. Each input ADC has a separate cancellation for each RX block channel.

### Front-end AGC

The feAGC block is used to control the RX ADC input level by controlling an external DVGA.

The feAGC has multiple channels in each RX block:

- 1 real stream up to  $4 \times$  DPD clock rate (only use one block)
- 2 real (using both blocks) or 1 complex stream (only use one block) up to  $2 \times$  DPD clock rate each
- 4 real or 2 complex streams up to DPD clock rate each (uses both blocks)
- 8 real or 4 complex streams up to  $1/2$  DPD clock rate each (uses both blocks)

The feAGC has both threshold comparison and an integrated power measurement. The feAGC has an error accumulation. The error accumulation can be mapped to a specific ADC desired operating point. The integral controller outputs the DVGA value to control the ADC input. DVGA controls are mapped to the specific DVGA outputs, supporting multiple DVGA types. Multipliers in the data path can be used to compensate for external DVGA gain changes (from the feAGC output control word). A delay block aligns the gain value applied to the internal multiplier with the point in time on the data samples where the external gain change was applied. Use of this multiplier minimizes gain steps that would cause transients in the downstream digital filters and allows relative power measurements on the digital signals.

The AGC operation may be suspended during certain conditions. The internal controlled-delay AGC update and special clock gating can be used to suspend the AGC operation.

The control word outputs from the feAGC blocks are applied to external DVGA parts via the DVGA pins. There are 16 DVGA pins (3.3-V CMOS) which may be individually configured as DVGA output signals or GPIO (input or output) signals. When used as DVGA control signals, there are two modes:

- Transparent mode – parallel output words are connected directly to DVGAs that are being used in a mode without a clock or latch signal to clock-in the gain word. This is the minimum latency mode. There can be two ports of 8 bits each, three ports of 5 bits each, four ports of 4 bits each, or five ports of 3 bits each.
- Clocked mode – eight latch enable (LE) signals and one 8-bit output word. This mode allows up to eight control signals, up to 8 bits each, but with increased latency. The LE signal may be a positive or negative pulse, with programmable width.

### R2C

In the real-to-complex conversion block, real signal inputs are up- or downconverted by  $f_s/4$ , filtered to isolate the selected sideband, and decimated by a factor of 2. Real-to-complex conversion is bypassed for complex inputs.

The rejection of the R2C decimation filter is:

- For 90% bandwidth signal, –68 dB, stop band
- For 80% bandwidth signal, –106 dB, stop band

**Switch**

Any of the up to eight complex RX antenna/signal inputs across both sub-chips may be switched to one or more of the up to 4 output streams of each sub-chip.

**IF NCO**

The NCO/mixer block generates in-phase and quadrature sinusoidal signals (cos/sin) and mixes them with the switched antenna streams to frequency-translate the RX signals. The NCO contains a 48-bit frequency word and 48-bit accumulator.

**BDC**

The BDC supports the following modes and sample rates at its input (across both sub-chips):

- Single –  $4 \times$  DPD clock rate real,  $2 \times$  DPD clock rate complex
- Dual –  $2 \times$  DPD clock rate real, DPD clock rate complex
- Quad – DPD clock rate real,  $1/2$  DPD clock rate complex
- Octal –  $1/2$  DPD clock rate real

Total decimation factors may be 1, 2, 4, 8, or 16. The decimation filtering is achieved with the cascade of the real-to-complex filter (R2C), a fixed filter F1, and a fixed filter F2. The rejection of the F1 and F2 filters is:

- Filter F1 (decimate by 1 or 2)
  - If used, always followed by filter F2, so relaxed requirements
  - 45% bandwidth,  $-107$  dB stopband
- Filter F2
  - Recirculated 1–3 times to provide 2, 4, or  $8 \times$  decimation factor
  - 90% bandwidth,  $-75$  dB, stop band
  - 80% bandwidth,  $-106$  dB, stop band

**Equalizer**

The receive equalizer is full-complex 16-tap filter that performs the following signal-processing functions:

- Programmable spectral inversion at the input
- Equalization of analog signal paths
- Channel equalization for repeater applications
- Gain/phase/fractional delay adjust (MIMO/smart antenna support)
- Fixed dc offset compensation at the output

Independent complex coefficients for real and imaginary signal data allow full flexibility for independent equalization of the direct- and cross-IQ signal components, as well as frequency-dependent IQ gain and phase imbalance compensation. The programmable 16-bit coefficient sets (i.e.,  $C_{ij}$ ,  $C_{qq}$ ,  $C_{iq}$  and  $C_{qi}$ , for each tap) can be updated on the fly.

**IQ imbalance correction**

Automatic correction of IQ imbalance is provided with a 1-tap blind adaptive algorithm. The correction coefficients also may be programmed to fixed values. This block supports programmable integration intervals and flexible gating of loop operation.

**RX Distributor**

The outputs from the RX sub-chips are routed to the RX distributor block, which enables arbitrary assignment of RX streams to DDC channels and blocks.

**RX Baseband Output Formatter**

The RX baseband (BB) output formatter block accepts data from the DDC and formats the data for output on the BB LVDS pins. A back-end AGC (beAGC) function is included that optionally adjusts the gain of each channel and provides multiple format options. There are 12 unidirectional LVDS pairs for the RX BB interface.

## Back-end AGC

The beAGC function is available for receive channels from DDUC3 and DDUC2 (DDUC1 and DDUC0 may also be used for receive—with the formats as described following—but without the beAGC function). When the floating-point format is selected (described following), the beAGC is not used. For the fixed-point formats, the beAGC may be on or off. There are separate beAGC blocks associated with DDUC3 and DDUC2, and each block can process up to 12 channels. Within a block, there are two sets of control parameters. This provides support for two different signal types sharing the same DDUC block. Each channel may have a programmable-gain starting point or a fixed gain, and there is a per-channel flexible gating signal to control freeze/operate intervals for TDD signal types. The beAGC has approximately a 100 dB dynamic range. The beAGC algorithm adjusts the gain to drive the median magnitude of gain-loop output data to a target threshold value. There are four step-sizes used (two for above and two for below the threshold), depending on distance from the threshold value.

## Output formatter

There are three operational modes for the RX BB output formatter: byte mode (B, 9 bits), nibble mode (N, 4 bits), and serial mode (S, 2 bits). The nibble and serial modes allow multiple BB output rates and the use of fewer pins on the interface. The GC533x can provide up to three different BB output data rates. [Table 7](#) and [Table 8](#) summarize the different modes and pin assignments for the byte, nibble, and serial modes. As can be seen in [Table 8](#), there are two data formats supported:

- Floating point (indicated with an F in the mode label; 14- or 16-bit mantissa, 4-bit exponent)
- Fixed point without gain word (16- or 18-bit options)

In [Table 8](#), BBOUT[X] is the BBOUT differential pair (assumed positive and negative connections), and BB0, BB1, and BB2 represent three different RX differential baseband input signals that can be at arbitrary rates.

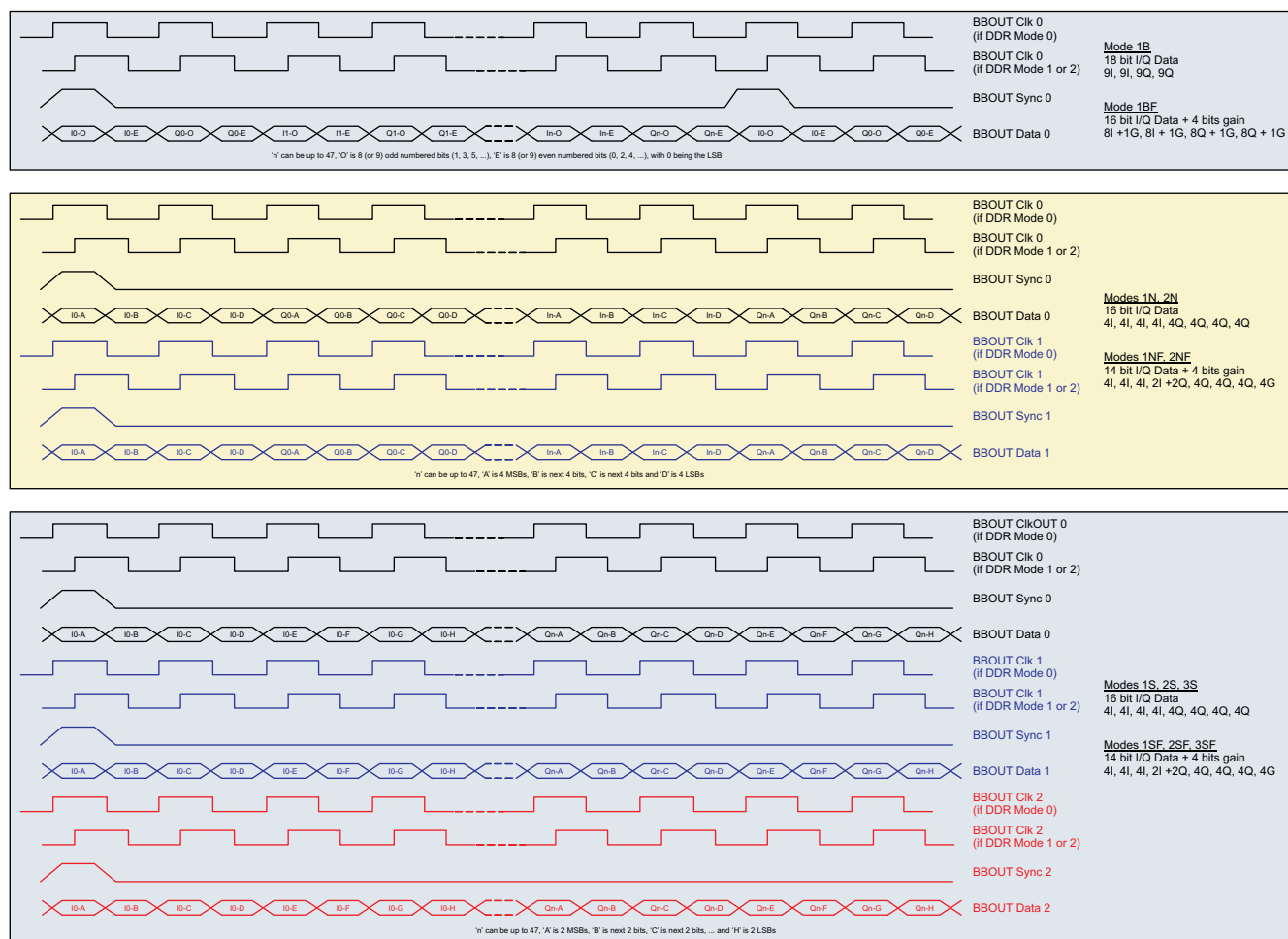
[Figure 13](#) shows the BB output formats. The maximum-data-rate configurations have the DDR clock out transitioning synchronously with the data (referred to as *DDR Mode 0* in the table). At half the maximum possible data rate (referred to as *DDR Mode 1* in the table) and a quarter of the maximum possible data rate (referred to as *DDR Mode 2* in the table), the DDR clock out transitions in the middle of the data-steady time .

**Table 7. RX BB Formatter Modes**

| MODE | Description                                          | Total Number of Interface Pins                                                         | Maximum Complex Interface Rate per Channel<br>N is the number of channels |
|------|------------------------------------------------------|----------------------------------------------------------------------------------------|---------------------------------------------------------------------------|
| 1B   | 1 interface rate (up to 18 bits)                     | 11 = 9 data + 1 clk + 1 sync                                                           | (Clk4/4)/N/2; maximum 125 MSPS total (for all channels)                   |
| 1BF  | 1 interface rate (up to 16 bits) + exponent (4 bits) | 10 = 8 data + 1 clk + 1 sync                                                           | (Clk4/4)/N/2; maximum 125 MSPS total (for all channels)                   |
| 1N   | 1 interface rate (16 bits)                           | 6 = 4 data + 1 clk + 1 sync                                                            | (Clk4/8)/N; maximum 96.15 (Nibble0), 125 (Nibble1) MSPS total             |
| 1NF  | 1 interface rate (14 bits) + exponent (4 bits)       | 6 = 4 data + 1 clk + 1 sync                                                            | (Clk4/8)/N; maximum 96.15 (Nibble0), 125 (Nibble1) MSPS total             |
| 1S   | 1 interface rate (16 bits)                           | 4 = 2 data + 1 clk + 1 sync                                                            | (Clk4/16)/N; maximum 48.07 MSPS total                                     |
| 1SF  | 1 interface rate (14 bits) + exponent (4 bits)       | 4 = 2 data + 1 clk + 1 sync                                                            | (Clk4/16)/N; maximum 48.07 MSPS total                                     |
| 2N   | 2 interface rates (16 bits)                          | 12 = 4 data + 1 clk + 1 sync +<br>4 data + 1 clk + 1 sync                              | (Clk4/8)/N; maximum 221.15 MSPS total                                     |
| 2NF  | 2 interface rates (14 bits) + exponent (4 bits)      | 12 = 4 data + 1 clk + 1 sync +<br>4 data + 1 clk + 1 sync                              | (Clk4/8)/N; maximum 221.15 MSPS total                                     |
| 2S   | 2 interface rates (16 bits)                          | 8 = 2 data + 1 clk + 1 sync +<br>2 data + 1 clk + 1 sync                               | (Clk4/16)/N; maximum 96.15 MSPS total                                     |
| 2SF  | 2 interface rates (14 bits)+ exponent (4 bits)       | 8 = 2 data + 1 clk + 1 sync +<br>2 data + 1 clk + 1 sync                               | (Clk4/16)/N; maximum 96.15 MSPS total                                     |
| 3S   | 3 interface rates (16 bits)                          | 12 = 2 data + 1 clk + 1 sync +<br>2 data + 1 clk + 1 sync +<br>2 data + 1 clk + 1 sync | (Clk4/16)/N; maximum 144.23 MSPS total                                    |
| 3SF  | 3 interface rates (14 bits)+ exponent (4 bits)       | 12 = 2 data + 1 clk + 1 sync +<br>2 data + 1 clk + 1 sync +<br>2 data + 1 clk + 1sync  | (Clk4/16)/N; maximum 144.23 MSPS total                                    |

Table 8. RX BB Pin Assignments

| LVDS Pair BBI[11:0]                               | Byte Mode  | Nibble Mode | Serial Mode |
|---------------------------------------------------|------------|-------------|-------------|
| BBOUT[0] pos. and neg.                            | BB0_DATA_0 | BB0_DATA_0  | BB0_DATA_0  |
| BBOUT[1] pos. and neg.                            | BB0_DATA_1 | BB0_DATA_1  | BB0_DATA_1  |
| BBOUT[2] pos. and neg.                            | BB0_DATA_2 | BB0_SYNC    | BB0_SYNC    |
| BBOUT[3] pos. and neg.                            | Spare      | BB0_CLOCK   | BB0_CLOCK   |
| BBOUT[4] pos. and neg.                            | BB0_DATA_3 | BB0_DATA_2  | BB1_DATA_0  |
| BBOUT[5] pos. and neg.                            | BB0_DATA_4 | BB0_DATA_3  | BB1_DATA_1  |
| BBOUT[6] pos. and neg.                            | BB0_SYNC   | BB1_SYNC    | BB1_SYNC    |
| BBOUT[7] pos. and neg.                            | BB0_CLOCK  | BB1_CLOCK   | BB1_CLOCK   |
| BBOUT[8] pos. and neg.                            | BB0_DATA_5 | BB1_DATA_0  | BB2_DATA_0  |
| BBOUT[9] pos. and neg.                            | BB0_DATA_6 | BB1_DATA_1  | BB2_DATA_1  |
| BBOUT[10] pos. and neg.                           | BB0_DATA_7 | BB1_DATA_2  | BB2_SYNC    |
| BBOUT[11] pos. and neg.                           | BB0_DATA_8 | BB1_DATA_3  | BB2_CLOCK   |
| Number of BBdata streams                          | 1          | 2           | 3           |
| Number of DDR clocks to transfer 1 complex sample | 2          | 4           | 8           |



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Figure 13. RX BB Formats

## Capture Buffers

The GC533x has two capture buffers, each 4096 complex words (18-bits I, 18-bits Q) deep, which are periodically read by the external coefficient update controller (DSP) in order to optimize the DPD coefficients. The capture buffers can be configured to sample data signals at the following points in the GC533x:

- DPD HP mode input (Referred to as node A)
- DPD HP mode output (Node B)
- DPD HB mode input (Node C)
- DPD HB mode output (Node D)
- RX AB input (Node E)
- RX path 0/1 output (Node F)
- RX C (feedback) input (Node G)
- Testbus

The capture buffers can be triggered via an external sync signal, through a software trigger, or when the monitored signal exceeds the user-configurable thresholds. The capture buffers can be programmed to monitor the signal statistics continuously and only capture data when certain requirements are met, as well as to generate an interrupt when a qualified buffer is captured. This helps in selecting an optimum set of data for the DSP to use in optimizing the DPD coefficients. The capture buffers can be read by the DSP via the MPU interface.

The capture buffers also allow synchronized multi-chip data capture. For a multiple antenna system that uses more than one GC533x, a feedback signal to use in adapting DPD coefficients in multiple GC533x chips can be connected to just one of the GC533x chips. The SYNCOUT signal can be used to daisy-chain (e.g., connecting to SYNCA on the next chip) across the GC533x chips in the system. The SYNCOUT signal indicates the end of the data capture and can be used as a capture trigger in all chips.

## Microprocessor (MPU) Interface

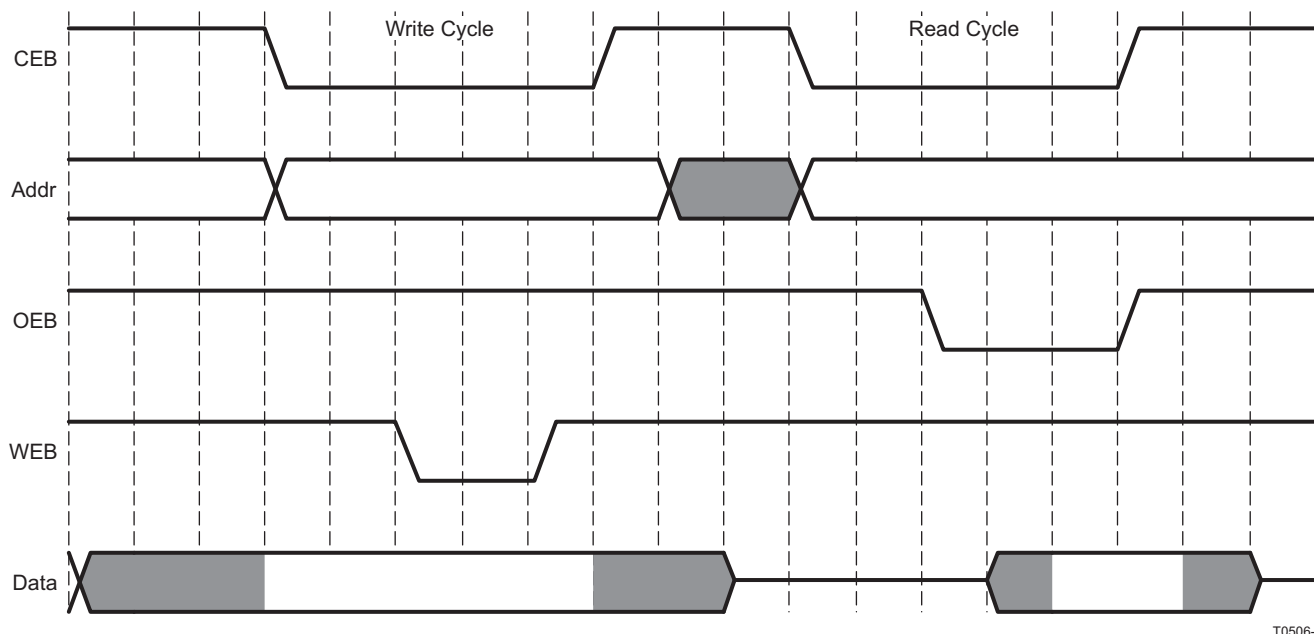
The MPU interface is designed to interface with external memory interface (EMIF) ports on TI DSPs operating in asynchronous mode. It consists of a 16-bit bidirectional data bus, an 8-bit address bus, and WEB, OEB, CEB, and EMIFENA control signals. The interface supports the TI 'C6748 as an EMIF asynchronous interface. The MPU interface has two address spaces: a paged address space and an auto-increment address space.

To enable the EMIF interface, pin EMIFENA must be set to logic high.

In an MPU write cycle, a GC533x internal MPUCLK signal is generated by NORing CEB and WEB. The MPUCLK signal goes high when both CEB and WEB are asserted and goes low as soon as either CEB or WEB is de-asserted. The MPU data is latched on the rising edge of the MPUCLK signal. For the auto-increment address spaces, the auto-increment address increments on the falling edge of the MPUCLK signal.

In an MPU read cycle, a GC533x internal MPUCLK signal is generated by NORing CEB and OEB. The MPUCLK signal goes high when both CEB and OEB are asserted and goes low as soon as either CEB or OEB is de-asserted. The MPU readback data is available soon after the rising edge of the MPUCLK signal. For the auto-increment address spaces, the auto-increment address increments on the failing edge of the MPUCLK signal.

[Figure 14](#) shows the MPU interface timing diagram. The timing specifications are provided in [Table 26](#) and [Table 27](#).



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Figure 14. MPU Interface Format

## Serial Peripheral Interface (SPI)

The MPU and SPI interfaces can be only enabled one at a time. EMIFENA must be set to logic low to enable the SPI interface. A three- or four-wire SPI interface is supported in the GC533x. It consists of SPIDENB, SPICLK, SPIDIO, and SPIDO-(SPARE) (output in four-wire mode) signals. See [Table 25](#) and [Figure 25](#).

## JTAG Interface

The GC533x includes a five-pin JTAG interface that supports boundary scan for all CMOS pads in the chip, aside from the TESTMOD pin. The BBIN, BBOU, RX, TX, and SYNC pins are all LVDS and do not get JTAG boundary scan. **IMPORTANT NOTE:** if not using JTAG, the TRSTB signal should be grounded (or pulled to ground through  $R \leq 1\text{ k}\Omega$ ); otherwise, the JTAG port may take control of the pins. See [Table 24](#) and [Figure 24](#).

A BSDL file is available on the GC533x Web page.

## Input and Output Syncs

The GC533x features two LVDS input syncs (SYNCA and SYNCB) and one LVDS output (SYNCOUT) user-programmable sync. These are typically used as trigger/synchronization mechanisms to activate features within the device. The input syncs can be used to trigger events such as:

- Power measurements
- DUC channel delay, mixer phase and dither
- Initializing/loading filter coefficients
- Capturing and sourcing of data in the capture buffers
- Controlling gating intervals for AGC and other adaptive loops
- Frequency NCO changes, or hopping synchronization

The SYNCA signal is used for device startup. The SYNCB signal can be used for shared feedback synchronization between multiple GC533x devices. The sync signal is active-high. The width (number of positive edges of the DPD clock) of the sync signal depends on the configuration. See the GC533x sync and MPU application note to determine the proper sync duration. A typical sync-pulse duration is four DPD clocks. The sync must be periodic, and usually starts at the beginning of the TX frame.

The output sync can be programmed to reflect triggering of specific events within the GC533x, and is primarily used to output the capture-buffer sync out signal.

## Programmable Power Meters

### Interval-Based Power Meter

There are three interval-based power meters which compute magnitude-squared sample values during programmable time intervals and provide the following results:

- Integrated magnitude-squared power
- Peak power
- Number of magnitude-squared values above a first threshold
- Number of magnitude-squared values above a second threshold

An interrupt bit is set when new measurement results are available. For its input, each power meter can independently select from the same set of internal node sources as the capture buffers.

### Running-Average Power Meter for PA Protection

The running-average power meter monitors up to four signal streams on a single node, which is selectable from the same set of internal sources as the capture buffers. For each signal stream, it measures running-average power and counts instantaneous power values above a threshold (referred to as *peaks*). It can be used in conjunction with hardware alarms for monitoring power levels for PA protection.

The running-average power meter has the following features:

- Running average mode, with programmable forgetting factor exponent,  $u$  ( $0 < u < 15$ )  

$$y(k+1) = (1 - 2^{-u}) \times y(k) + 2^{-u} \times |x(k)|^2,$$
where  $x(k)$  is the signal sample and  $y(k)$  is the power meter output.  
Typically, one must set  $u = 11$  to get 0.5-dB accuracy,  $u = 14$  to get 0.1-dB accuracy.
- Peak count mode: counts the number of power values,  $|x(k)|^2$ , above a threshold in a specified number of samples (*window*). The number of power values, threshold, and window are all programmable.
- Flexible gating of the operation interval

### Alarms

The output,  $y(k)$ , from the running-average power meter can be compared on an ongoing basis to programmable high and low thresholds (always positive). There are two alarms, *alarm0* and *alarm1*. Each alarm is triggered (if it is enabled) based on the programmed mode:

- (0) Disabled
- (1) Average power alarm. The alarm is triggered based on the following conditions:
  - If alarm polarity = 0 (see the *alm\_polarity* register),  $y(k) > \text{high\_threshold}$
  - If alarm polarity = 1,  $y(k) < \text{low\_threshold}$
  - If alarm polarity = 2,  $y(k) > \text{high\_threshold}$  or  $y(k) < \text{low\_threshold}$
- (2) Peak power alarm. The alarm is triggered based on the following conditions:
  - If the count of power values  $|x(k)|^2 > \text{peak\_threshold}$  exceeds the programmed number of samples, *peak\_samples*, in a programmed window, *peak\_window*
- (3) The alarm is triggered if either (1) or (2) occurs.

Alarm checks are computed on a per-antenna-stream basis. Each antenna stream  $y(k)$  result is compared to per-stream programmable thresholds.

Once an alarm has been triggered, the output INTERRPT pin is asserted and the appropriate (*alarm0* or *alarm1*) alarm interrupt bit is set and, for *alarm1*, a programmable action takes place. The programmable action is the same for all antenna streams, but the alarm triggering is independent for each antenna stream.

Programmable trigger actions for alarm1:

- (0) No action
- (1) Reduce gain of DPD output by programmable scale factor (programmed with stream[n].gain\_reduce), only if alarm caused by  $y(k) > \text{high\_threshold}$  and  $\text{alm\_polarit} = 0$  or  $2$ . The gain reduction is applied at the CFR input. A control signal from the capture buffer block is used to select the programmed gain value for the multiplier at the CFR input. When the host resets this alarm by writing to the appropriate register, the control signal returns to 0 (state that is not selecting the programmed gain value).

## GENERAL SPECIFICATIONS

### General Electrical Characteristics

This section describes the electrical characteristics for the CMOS interfaces (DVGA, MPU, JTAG, SPI, TESTMOD, RESETB and INTERRPT) and LVDS interfaces (BBIN, BBOUT, TXA, TXB, RXA, RXB, RXC, SYNC, DPDCLK) over recommended operating conditions (unless otherwise noted).

**Table 9. General Electrical Characteristics, CMOS Interface**

| PARAMETER                    | TEST CONDITIONS                               | MIN | NOM | MAX         | UNIT          |
|------------------------------|-----------------------------------------------|-----|-----|-------------|---------------|
| $V_{IL}$ Voltage input low   | See <sup>(1)</sup>                            |     |     | 0.8         | V             |
| $V_{IH}$ Voltage input high  | See <sup>(1)</sup>                            | 2   |     | $V_{DDSHV}$ | V             |
| $V_{OL}$ Voltage output low  | $I_{OL} = 2 \text{ mA}$ <sup>(1)</sup>        |     |     | 0.5         | V             |
| $V_{OH}$ Voltage output high | $I_{OH} = -2 \text{ mA}$ <sup>(1)</sup>       | 2.4 |     | $V_{DDSHV}$ | V             |
| $ I_{PU} $ Pullup current    | $V_{IN} = 0 \text{ V}$ <sup>(1)</sup>         | 30  | 100 | 250         | $\mu\text{A}$ |
| $ I_{PD} $ Pulldown current  | $V_{IN} = V_{DDSHV}$ <sup>(1)</sup>           | 30  | 100 | 250         | $\mu\text{A}$ |
| $ I_{IN} $ Leakage current   | $V_{IN} = 0$ or $V_{DDSHV}$ <sup>(1)(2)</sup> |     |     | 20          | $\mu\text{A}$ |

- (1) Chip specifications are production tested at 90°C case temperature for the given specification. Early production lots are sample tested at -40°C.
- (2) For inputs with no pullup or pulldown, inputs with pullup and  $V_{IN} = V_{DDSHV}$ , inputs with pulldown and  $V_{IN} = 0$ , and bidirectionals in input mode in either state.

**Table 10. General Electrical Characteristics, LVDS Interfaces**

| PARAMETER                                           | TEST CONDITIONS    | MIN  | NOM  | MAX  | UNIT     |
|-----------------------------------------------------|--------------------|------|------|------|----------|
| $V_{ICM}$ Input common mode voltage $(V_P - V_N)/2$ | See <sup>(1)</sup> | 700  |      | 1500 | mV       |
| $ V_P - V_N $ Input differential voltage            | See <sup>(1)</sup> | 150  |      | 700  | mV       |
| $R_{IN}$ Input differential impedance               | See <sup>(1)</sup> | 80   | 92   | 120  | $\Omega$ |
| $V_{COM}$ Output common-mode voltage                | See <sup>(2)</sup> | 1125 | 1200 | 1275 | mV       |
| $V_{OD}$ Output differential voltage                | See <sup>(1)</sup> | 250  |      | 500  | mV       |

- (1) Chip specifications are production tested at 90°C case temperature for the given specification. Early production lots are sample tested at -40°C.
- (2) Characteristics are determined by design.

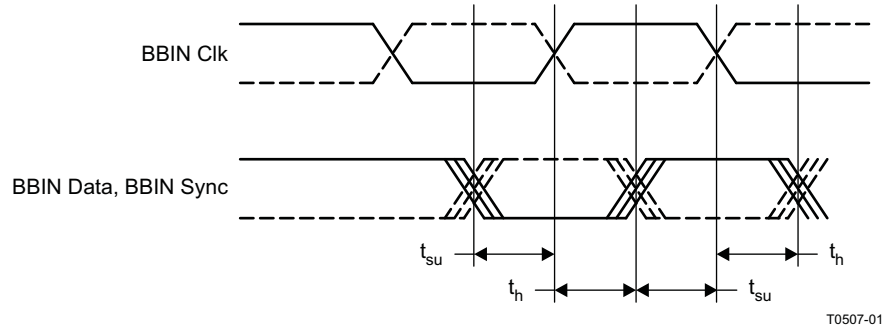
### General Switching Characteristics

The baseband interface TX has a single DDR interface input mode. The customer logic and trace routing must meet the listed  $t_{su}$  and  $t_h$  input timing.

**Table 11. General Switching Characteristics, TX BB LVDS Input**

| PARAMETER                          |                                              | TEST CONDITIONS       | MIN | NOM | MAX                          | UNIT |
|------------------------------------|----------------------------------------------|-----------------------|-----|-----|------------------------------|------|
| <b>BASEBAND INTERFACE DDR LVDS</b> |                                              |                       |     |     |                              |      |
| $f_{CLK(BB-Serial)}$               | Baseband input clock frequency               | See <sup>(1)</sup>    |     |     | 384                          | MHz  |
| $f_{CLK(BB-Nibble)}$               |                                              |                       |     |     | 500(Nibble0)<br>384(Nibble1) |      |
| $f_{CLK(BB-Byte)}$                 |                                              |                       |     |     | 384                          |      |
| $f_{CLK(RXA)}$                     | Baseband input clock frequency, using RXA    | See <sup>(1)</sup>    |     |     | 250                          | MHz  |
| $t_{su(BBS0)}$                     | BBIN3 Clk, BBIN1:0 Data, BBIN2 Sync          | See <sup>(1)(2)</sup> | 250 |     |                              | ps   |
| $t_{hi(BBS0)}$                     | BBIN3 Clk, BBIN1:0 Data, BBIN2 Sync          | See <sup>(1)(2)</sup> | 200 |     |                              | ps   |
| $t_{su(BBS1)}$                     | BBIN7 Clk, BBIN5:4 Data, BBIN6 Sync          | See <sup>(1)(2)</sup> | 210 |     |                              | ps   |
| $t_{hi(BBS1)}$                     | BBIN7 Clk, BBIN5:4 Data, BBIN6 Sync          | See <sup>(1)(2)</sup> | 250 |     |                              | ps   |
| $t_{su(BBS2)}$                     | BBIN11 Clk, BBIN9:8 Data, BBIN10 Sync        | See <sup>(1)(2)</sup> | 240 |     |                              | ps   |
| $t_{hi(BBS2)}$                     | BBIN11 Clk, BBIN9:8 Data, BBIN10 Sync        | See <sup>(1)(2)</sup> | 190 |     |                              | ps   |
| $t_{su(BBN0)}$                     | BBIN3 Clk, BBIN5,4,1,0 Data, BBIN2 Sync      | See <sup>(1)(2)</sup> | 250 |     |                              | ps   |
| $t_{h(BBN0)}$                      | BBIN3 Clk, BBIN5,4,1,0 Data, BBIN2 Sync      | See <sup>(1)(2)</sup> | 220 |     |                              | ps   |
| $t_{su(BBN1)}$                     | BBIN7 Clk, BBIN11:8 Data, BBIN6 Sync         | See <sup>(1)(2)</sup> | 250 |     |                              | ps   |
| $t_{h(BBN1)}$                      | BBIN7 Clk, BBIN11:8 Data, BBIN6 Sync         | See <sup>(1)(2)</sup> | 220 |     |                              | ps   |
| $t_{su(BB)}$                       | BBIN7 Clk, BBIN11:8,5:4,2:0 Data, BBIN6 Sync | See <sup>(1)(2)</sup> | 280 |     |                              | ps   |
| $t_{h(BB)}$                        | BBIN7 Clk, BBIN11:8,5:4,2:0 Data, BBIN6 Sync | See <sup>(1)(2)</sup> | 250 |     |                              | ps   |

- (1) Chip specifications are production tested at 90°C case temperature for the given specification. Early production lots are sample tested at –40°C.
- (2) Setup and hold times are measured from differential data crossing zero to differential clock crossing zero.



**Figure 15. TX Baseband LVDS Input Timing Specifications**

The BB LVDS RX outputs have three different output timing modes, DDR0, DDR1 and DDR2. DDR1 and DDR2 modes output data, and the BBclk output is centered over the data. In DDR0 mode, the data and clock are edge-aligned. Different BBOUT pins are used for clock, frame, and data pins depending on the byte, nibble, and serial modes. The DDR1 and DDR2 modes are shown in [Table 12](#) and [Figure 16](#). The DDR0 mode is shown in [Table 13](#) and [Figure 17](#). [Table 12](#) and [Figure 16](#). DDR1 mode is used upto a BBclk frequency of 310 MHz. DDR2 mode is used upto a BBclk frequency of 155 MHz. When the data rate is higher than 500 MHz, BBclk above 250 MHz, the operating mode is DDR0. In this mode, the clock is aligned with the output data transition. In DDR0 mode, the customer must delay the clock to meet the  $t_{su}$  and  $t_{hi}$  target for the baseband input. The  $t_{skw}$  time is measured as the relative skew for the data and frame to the clock output. This is shown in [Figure 13](#) and [Table 17](#).

In receive (uplink) mode, the GC5330 outputs data using the LVDS pins BBOUT. The BBOUT port may be operated in three modes, DDR0, DDR1, and DDR2.

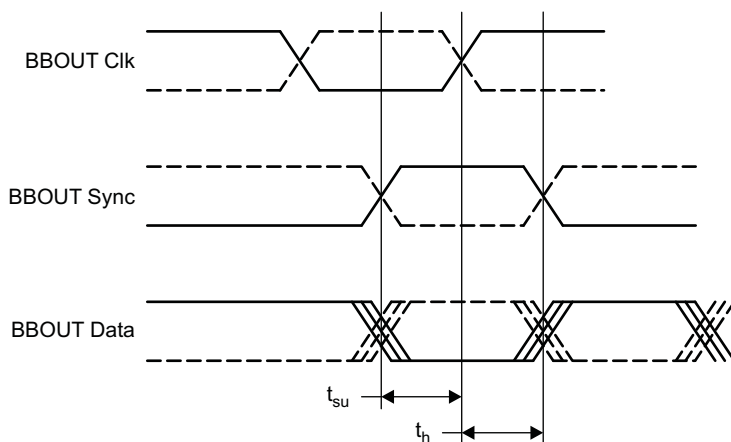
The lowest-rate outputs use DDR2 mode, where the output clock changes on one rising edge of the internal clock and the output data changes on the subsequent rising edge. In DDR2 mode, the output bit rate (per LVDS pair) is half of the internal clock. Middle-rate outputs use DDR1 mode, where the output clock changes on the falling edge of the internal clock and the output data changes on the rising edge of the internal clock, which results in an output bit rate equal to the internal clock rate. Both DDR1 and DDR2 result in the output clock edge occurring in the middle of output data-stable time. The DDR1 and DDR2 modes are shown in [Table 12](#) and [Figure 16](#).

The highest-rate outputs use DDR0 mode, where both the output clock and output data change with both the rising and falling edges of the internal clock. The DDR0 output bit rate is twice the internal clock rate. DDR0 results in the clock and data changing at the same time, and typically requires extra trace length on the PC board for the clockout signal to provide the required setup time for the receiving chip. The DDR0 mode is shown in [Table 13](#) and [Figure 17](#).

**Table 12. General Switching Characteristics, RX BB LVDS Output – DDR1, DDR2**

| PARAMETER                          |                                                 | TEST CONDITIONS                                               | MIN | NOM | MAX | UNIT |
|------------------------------------|-------------------------------------------------|---------------------------------------------------------------|-----|-----|-----|------|
| <b>BASEBAND INTERFACE DDR LVDS</b> |                                                 |                                                               |     |     |     |      |
| $f_{CLK(BB-DDR2)}$                 | Baseband output clock frequency                 | See <sup>(1)</sup> . Applies to BBOUT byte, nibble, or serial |     |     | 155 | MHz  |
| $f_{CLK(BB-DDR1)}$                 |                                                 |                                                               |     |     | 310 |      |
| $t_{skmin(BB)Serial0}$             | BBOUT3 Clk, BBOUT1:0 Data, BBOUT2 Sync          | See <sup>(2)(3)</sup>                                         |     | -20 |     | ps   |
| $t_{skmax(BB)Serial0}$             | BBOUT3 Clk, BBOUT1:0 Data, BBOUT2 Sync          | See <sup>(2)(3)</sup>                                         |     | 350 |     | ps   |
| $t_{skmin(BB)Serial1}$             | BBOUT7 Clk, BBOUT5:4 Data, BBOUT6 Sync          | See <sup>(2)(3)</sup>                                         |     | 15  |     | ps   |
| $t_{skmax(BB)Serial1}$             | BBOUT7 Clk, BBOUT5:4 Data, BBOUT6 Sync          | See <sup>(2)(3)</sup>                                         |     | 310 |     | ps   |
| $t_{skmin(BB)Serial2}$             | BBOUT11 Clk, BBOUT9:8 Data, BBOUT10 Sync        | See <sup>(2)(3)</sup>                                         |     | 60  |     | ps   |
| $t_{skmin(BB)Serial2}$             | BBOUT11 Clk, BBOUT9:8 Data, BBOUT10 Sync        | See <sup>(2)(3)</sup>                                         |     | 300 |     | ps   |
| $t_{skmax(BB)Nibble0}$             | BBOUT3 Clk, BBOUT5,4,1,0 Data, BBOUT2 Sync      | See <sup>(2)(3)</sup>                                         |     | 170 |     | ps   |
| $t_{skmax(BB)Nibble0}$             | BBOUT3 Clk, BBOUT5,4,1,0 Data, BBOUT2 Sync      | See <sup>(2)(3)</sup>                                         |     | 340 |     | ps   |
| $t_{skmin(BB)Nibble1}$             | BBOUT7 Clk, BBOUT11:8 Data, BBOUT6 Sync         | See <sup>(2)(3)</sup>                                         |     | 55  |     | ps   |
| $t_{skmax(BB)Nibble1}$             | BBOUT7 Clk, BBOUT11:8 Data, BBOUT6 Sync         | See <sup>(2)(3)</sup>                                         |     | 305 |     | ps   |
| $t_{skmin(BB)Byte}$                | BBOUT7 Clk, BBOUT11:8,5:4,2:0 Data, BBOUT6 Sync | See <sup>(2)(3)</sup>                                         |     | 250 |     | ps   |
| $t_{skmax(BB)Byte}$                | BBOUT7 Clk, BBOUT11:8,5:4,2:0 Data, BBOUT6 Sync | See <sup>(2)(3)</sup>                                         |     | 255 |     | ps   |

- (1) Chip specifications are production tested at 90°C case temperature for the given specification. Early production lots are sample tested at -40°C.
- (2) Skew measured for RX BBOUT data and frame signals, relative to the BBclk signal at zero crossing. BBclk is measured at threshold crossing. Lab measurement +signal → 50 Ω → Vcommon → 50 Ω → -signal. Vcommon has a 0.01-μF filter capacitor to GND. Differential probe used for measurement.
- (3)  $t_{su}$  calculation: 1/4 BBclk period -  $t_{skmin}$ ;  $t_h$  calculation: 1/4 BBclk period -  $t_{skmax}$



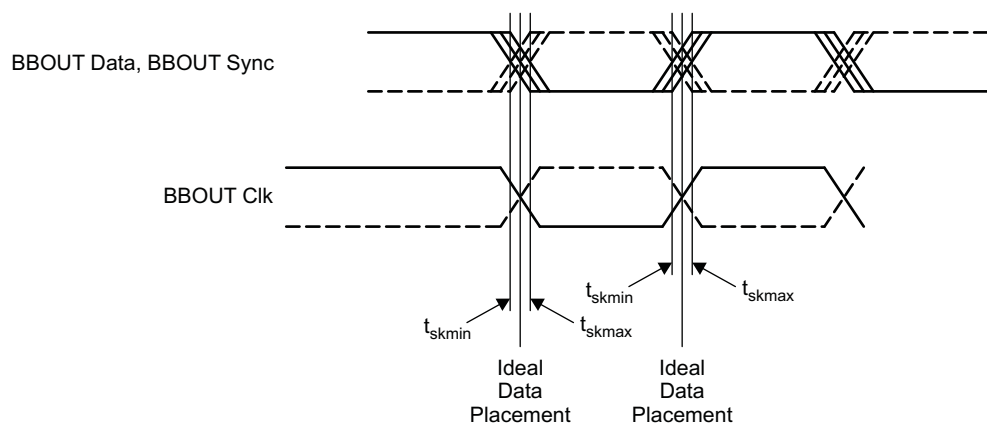
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**Figure 16. RX Baseband LVDS DDR1, DDR2 Output Timing Specifications**

**Table 13. General Switching Characteristics, RX BB LVDS Output – DDR0**

| PARAMETER                          |                                                 | TEST CONDITIONS          | MIN | NOM  | MAX | UNIT |
|------------------------------------|-------------------------------------------------|--------------------------|-----|------|-----|------|
| <b>BASEBAND INTERFACE DDR LVDS</b> |                                                 |                          |     |      |     |      |
| f <sub>CLK(Byte)</sub>             | Baseband output clock frequency                 | See <sup>(1)</sup>       |     |      | 384 | MHz  |
| f <sub>CLK(Nibble0)</sub>          |                                                 |                          |     |      | 384 | MHz  |
| f <sub>CLK(Nibble1)</sub>          |                                                 |                          |     |      | 500 | MHz  |
| f <sub>CLK(Serial)</sub>           |                                                 |                          |     |      | 384 | MHz  |
| t <sub>skmax(BB)Serial0</sub>      | BBOUT3 Clk, BBOUT1:0 Data, BBOUT2 Sync          | See <sup>(2)(3)</sup>    |     | –60  |     | ps   |
| t <sub>skmin(BB)Serial0</sub>      | BBOUT3 Clk, BBOUT1:0 Data, BBOUT2 Sync          | See <sup>(2)(3)(4)</sup> |     | 400  |     | ps   |
| t <sub>skmax(BB)Serial1</sub>      | BBOUT3 Clk, BBOUT1:0 Data, BBOUT2 Sync          | See <sup>(2)(3)</sup>    |     | –130 |     | ps   |
| t <sub>skmin(BB)Serial1</sub>      | BBOUT3 Clk, BBOUT1:0 Data, BBOUT2 Sync          | See <sup>(2)(3)(4)</sup> |     | 500  |     | ps   |
| t <sub>skmax(BB)Serial2</sub>      | BBOUT7 Clk, BBOUT5:4 Data, BBOUT6 Sync          | See <sup>(5)(6)</sup>    |     | –45  |     | ps   |
| t <sub>skmin(BB)Serial2</sub>      | BBOUT7 Clk, BBOUT5:4 Data, BBOUT6 Sync          | See <sup>(5)(6)(7)</sup> |     | 425  |     | ps   |
| t <sub>skmax(BB)Nibble0</sub>      | BBOUT3 Clk, BBOUT5,4,1,0 Data, BBOUT2 Sync      | See <sup>(5)(6)</sup>    |     | 0    |     | ps   |
| t <sub>skmin(BB)Nibble0</sub>      | BBOUT3 Clk, BBOUT5,4,1,0 Data, BBOUT2 Sync      | See <sup>(5)(6)(7)</sup> |     | 400  |     | ps   |
| t <sub>skmax(BB)Nibble1</sub>      | BBOUT7 Clk, BBOUT11:8 Data, BBOUT6 Sync         | See <sup>(5)(6)</sup>    |     | 10   |     | ps   |
| t <sub>skmin(BB)Nibble1</sub>      | BBOUT7 Clk, BBOUT11:8 Data, BBOUT6 Sync         | See <sup>(5)(6)(7)</sup> |     | 460  |     | ps   |
| t <sub>skmax(BB)Byte</sub>         | BBOUT7 Clk, BBOUT11:8,5:4,2:0 Data, BBOUT6 Sync | See <sup>(5)(6)</sup>    |     | 0    |     | ps   |
| t <sub>skmin(BB)Byte</sub>         | BBOUT7 Clk, BBOUT11:8,5:4,2:0 Data, BBOUT6 Sync | See <sup>(5)(6)(7)</sup> |     | 480  |     | ps   |

- (1) Chip specifications are production tested at 90°C case temperature for the given specification. Early production lots are sample tested at –40°C.
- (2) Skew measured for RX BBOUT data and frame signals, relative to the BBclk signal at zero crossing. BBclk is measured at threshold crossing. Lab measurement +signal → 50 Ω → Vcommon → 50 Ω → –signal. Vcommon has a 0.01-μF filter capacitor to GND. Differential probe used for measurement.
- (3) The customer interface design modifies the trace lengths based on the desired receiver timing and clock delays.
- (4) t<sub>su</sub> = –t<sub>skmax</sub>; t<sub>hold</sub> = 1/4 BBclk period – t<sub>skmin</sub>.
- (5) Skew measured for RX BBOUT data and frame signals, relative to the BBclk signal at zero crossing. BBclk is measured at threshold crossing. Lab measurement +signal → 50 Ω → Vcommon → 50 Ω → –signal. Vcommon has a 0.01-μF filter capacitor to GND. Differential probe used for measurement.
- (6) The customer interface design modifies the trace lengths based on the desired receiver timing and clock delays.
- (7) t<sub>su</sub> = –t<sub>skmax</sub>; t<sub>hold</sub> = 1/4 BBclk period – t<sub>skmin</sub>.



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**Figure 17. RX Baseband LVDS DDR0 Output Timing Specifications**

The DAC TX interface has a 40-signal output bus. The DAC TX bus can provide 4-byte-wide or 2-word-wide interfaces. [Table 5](#) shows the different DAC devices that can be connected to the TX output ports. The DAC TX interface has two styles of clock output, one where the DDR clock is centered over the output data-stable time, and one where the clock transition is aligned with the data transition. If the output clock rate is greater than 500 MHz, the GC533x must be configured for clock transition aligned with the data transition. Depending on the DAC type selected, the clock, frame, and data for the DAC may require a trace routing delay for proper alignment. See [Table 14](#), [Table 15](#), and [Table 16](#).

**Table 14. TX DAC and Envelope Modulator Characteristics**

| DAC or Envelope Modulator Type        | Timing Model                                                                                                             | DAC Data Rate | Table Number             | Figure Number             |
|---------------------------------------|--------------------------------------------------------------------------------------------------------------------------|---------------|--------------------------|---------------------------|
| DAC3282, 3283 byte-envelope modulator | Clock centered over data                                                                                                 | <1000 Mbyte/s | <a href="#">Table 15</a> | <a href="#">Figure 18</a> |
| DAC3282, 3283 byte-envelope modulator | Clock aligned with data at GC533x, routing provides timing skew for clock centered over data                             | ≥1000 Mbyte/s | <a href="#">Table 16</a> | <a href="#">Figure 19</a> |
| DAC3484, 3482 word                    | Clock centered over data                                                                                                 | <1000 Mword/s | <a href="#">Table 15</a> | <a href="#">Figure 18</a> |
| DAC3484, 3482 word                    | Clock aligned with data at GC533x, routing provides timing skew for clock centered over data                             | ≥1000 Mword/s | <a href="#">Table 16</a> | <a href="#">Figure 19</a> |
| DAC5682                               | Clock aligned with data at GC533x. PC board routing may be required to provide some timing skew for optimum performance. | All           | <a href="#">Table 16</a> | <a href="#">Figure 19</a> |

**Table 15. TX DAC Clock Centered Over Data Switching Characteristics (See Table 5 for Connections)**

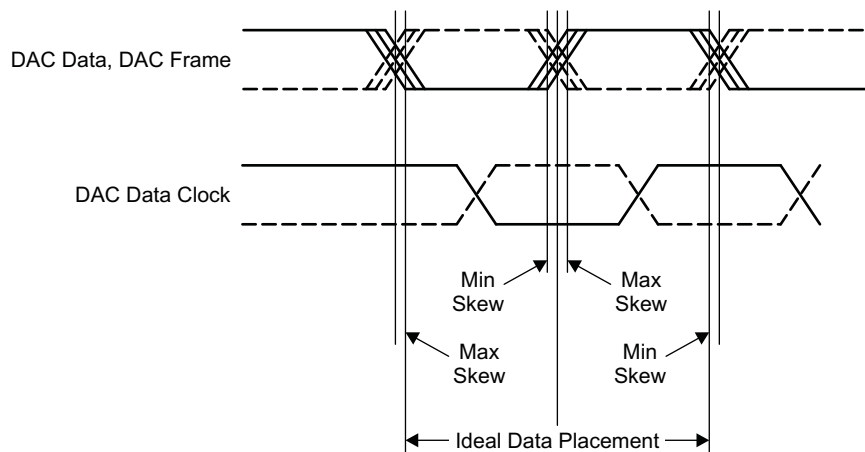
| PARAMETER       |                            | TEST CONDITIONS       | MIN      | MAX      | UNIT |
|-----------------|----------------------------|-----------------------|----------|----------|------|
| <b>DDR LVDS</b> |                            |                       |          |          |      |
| $f_{CLK(DAC)}$  | DAC output clock frequency | See <sup>(1)</sup>    |          | 620      | MHz  |
| CLOCK           | DATA                       | TEST CONDITIONS       | MIN SKEW | MAX SKEW | UNIT |
| TXA4            | TXA9:5, 3:0                | See <sup>(2)(3)</sup> | –190     | 139      | ps   |
| TXA14           | TXA19:15, 13:10            | See <sup>(2)(3)</sup> | –241     | 205      | ps   |
| TXA9            | TXA19:10, 8:0              | See <sup>(2)(3)</sup> | –200     | 155      | ps   |
| TXB4            | TXB9:5, 3:0                | See <sup>(2)(3)</sup> | –169     | 238      | ps   |
| TXB14           | TXB19:15, 13:10            | See <sup>(2)(3)</sup> | –198     | 146      | ps   |
| TXB9            | TXB19:10, 8:0              | See <sup>(2)(3)</sup> | –145     | 235      | ps   |

- (1) Chip specifications are production tested at 90°C case temperature for the given specification. Early production lots are sample tested at –40°C.
- (2) Skew measured from DAC DATA desired P/N crossing to DATA P/N crossing. A negative skew is when the data arrives prior to the clock.
- (3)  $t_{su} = 1/4$  DAC clock period – Max. Skew,  $t_h = 1/4$  DAC clock period + Min. Skew

**Table 16. TX DAC Clock Aligned With Data Switching Characteristics (See Table 5 for Connections)**

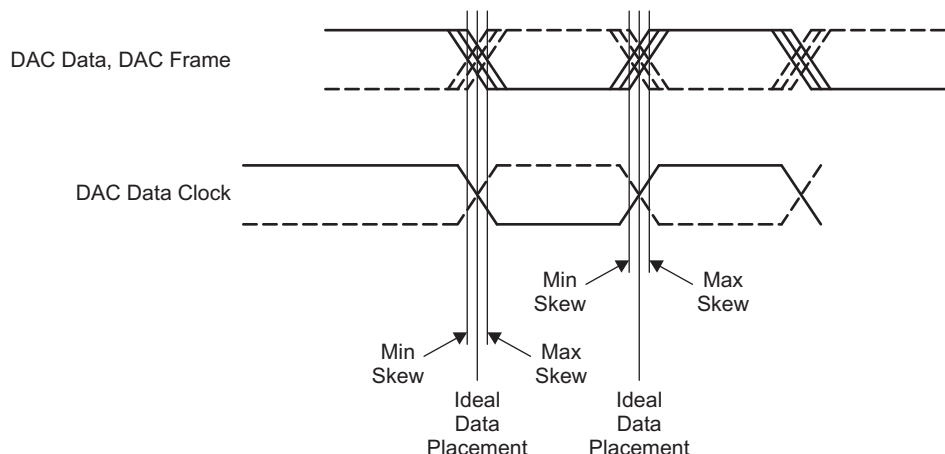
| PARAMETER       |                            | TEST CONDITIONS    | MIN      | MAX      | UNIT |
|-----------------|----------------------------|--------------------|----------|----------|------|
| <b>DDR LVDS</b> |                            |                    |          |          |      |
| $f_{CLK(DAC)}$  | DAC output clock frequency | See <sup>(1)</sup> |          | 620      | MHz  |
| CLOCK           | DATA                       | TEST CONDITIONS    | MIN SKEW | MAX SKEW | UNIT |
| TXA4            | TXA9:5, 3:0                | See <sup>(2)</sup> | –190     | 139      | ps   |
| TXA14           | TXA19:15, 13:10            | See <sup>(2)</sup> | –241     | 205      | ps   |
| TXA9            | TXA19:10, 8:0              | See <sup>(2)</sup> | –200     | 155      | ps   |
| TXB4            | TXB9:5, 3:0                | See <sup>(2)</sup> | –169     | 238      | ps   |
| TXB14           | TXB19:15, 13:10            | See <sup>(2)</sup> | –198     | 146      | ps   |
| TXB9            | TXB19:10, 8:0              | See <sup>(2)</sup> | –145     | 235      | ps   |

- (1) Chip specifications are production tested at 90°C case temperature for the given specification. Early production lots are sample tested at –40°C.
- (2) Skew measured from DAC DATA desired P/N crossing to DATA P/N crossing. A negative skew is when the data arrives prior to the clock.



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**Figure 18. TX LVDS Timing Specifications (TXA and TXB) (DACCLK Centered Over Data)**



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**Figure 19. TX LVDS Timing Specifications (TXA and TXB) (DACCLK Aligned With Data)**

The envelope modulator interface uses the same pins as the DAC interface. The ET connections are shown in [Table 5](#). The ET modulator timing is listed in [Table 15](#).

Data is output most-significant byte (half-word) first with the rising edge of the clockout in the middle of data-stable time, then least-significant byte (half-word) with the falling edge of the clockout in the middle of the data-stable time.

The ADC output interface has two types of timing, based on the clock centered over the data, or clock edge-aligned with the data. The GC533x only processes clock centered over the data. Each ADC type is characterized by the data and clock alignment, in [Table 17](#), from which the proper table and timing diagram can be determined as follows: ADC W7 in [Table 18](#) and [Figure 20](#); ADC W14 in [Table 19](#) and [Figure 21](#); and ADC B7 in [Table 20](#) and [Figure 20](#). Note: The general ADC routing is to align the clock and data traces with a common routing delay. For the ADS5463 and ADS5474 the clock trace must be adjusted in length to meet the system timing design.

Note: when RXA is used as a baseband interface, the specification is shown in [Table 17](#). The table shows a sampling of ADCs released at publication time. If the clock is not centered, the pc board may require added routing delay to the clock out to satisfy the setup time requirements. See (\*) in [Table 17](#).

W7 – word-wide ADC interface, clock on bit 7

W14 – word-wide ADC interface, clock on bit 14

B7 – byte-wide ADC interface, clock on bit 7

B14 – byte-wide ADC interface, clock on bit 14

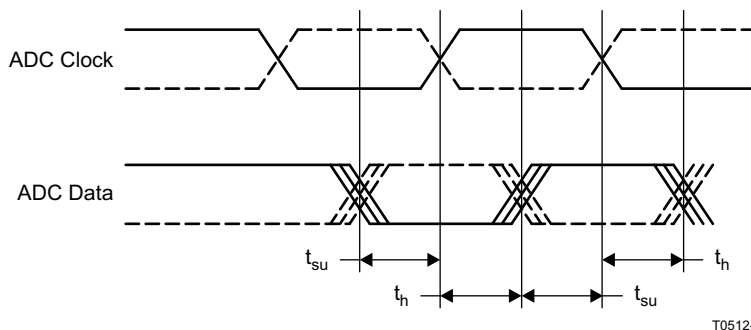
**Table 17. General LVDS ADC Interface Table**

| ADC Type                   | Bits per Rail | Clock Centered | ADC Format            | ADC Input Timing Table | ADC Figure |
|----------------------------|---------------|----------------|-----------------------|------------------------|------------|
| ADS5400                    | 1             | Yes            | W7                    | Table 18               | Figure 20  |
| ADS54RF63 (*)              | 1             | No             | W14                   | Table 19               | Figure 20  |
| ADS5463 (*)                | 1             | No             | W14                   | Table 19               | Figure 20  |
| ADS5474 (*)                | 1             | No             | W14                   | Table 19               | Figure 20  |
| RXA as baseband TX input   | 2             | Yes            | Baseband format – W14 | Table 21               | Figure 20  |
| ADS61xx, ADS41xx, ADS62pxx | 2             | Yes            | B7                    | Table 20               | Figure 20  |
| ADS55xx                    | 2             | Yes            | B7, W7                | Table 20Table 18       | Figure 20  |
| ADS58B18                   | 2             | Yes            | B7, W7                | Table 20Table 18       | Figure 20  |
| ADS58B28, ADS62c1x         | 2             | Yes            | B7, W7                | Table 20Table 18       | Figure 20  |
| ADS64xx                    | 6 or 7        | Yes            | W7                    | Table 18               | Figure 21  |
| ADS52xx                    | 12 or 14      | Yes            | W7                    | Table 18               | Figure 21  |

**Table 18. RX ADC-W7 Switching Characteristics**

| PARAMETER                                                                   | TEST CONDITIONS | MIN | NOM | MAX | UNIT |
|-----------------------------------------------------------------------------|-----------------|-----|-----|-----|------|
| $f_{CLK(ADC)}$ RX input clock frequency, ADCA7 Clk                          | See (1)         |     |     | 620 | MHz  |
| $t_{su(ADC,A)}$ Input data setup time on port A before ADCA7 Clk transition | See (1)(2)      | 260 |     |     | ps   |
| $t_{h(ADC,A)}$ Input data hold time on port A after ADCA7 Clk transition    | See (1)(2)      | 170 |     |     | ps   |
| $t_{su(ADC,B)}$ Input data setup time on port B before ADCB7 Clk transition | See (1)(2)      | 260 |     |     | ps   |
| $t_{h(ADC,B)}$ Input data hold time on port B after ADCB7 Clk transition    | See (1)(2)      | 140 |     |     | ps   |

- (1) Chip specifications are production tested at 90°C case temperature for the given specification. Early production lots are sample tested at –40°C.
- (2) Setup and hold times apply to data and appropriate ADC Clk, respectively. Timing is measured from ADC Clk threshold crossing.


**Figure 20. RX ADC LVDS Timing Specifications (RXA and RXB)**

**Table 19. RX ADC-W14 Switching Characteristics**

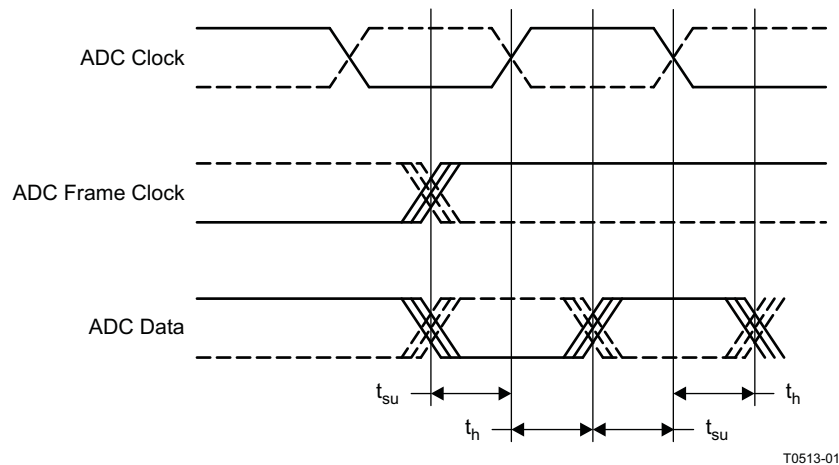
| PARAMETER       |                                                              | TEST CONDITIONS       | MIN | NOM | MAX | UNIT |
|-----------------|--------------------------------------------------------------|-----------------------|-----|-----|-----|------|
| $f_{CLK(ADC)}$  | RX input clock frequency ADCA14 Clk, ADCB14 Clk              | See <sup>(1)</sup>    |     |     | 620 | MHz  |
| $t_{su(ADC,A)}$ | Input data setup time on port A before ADCA14 Clk transition | See <sup>(1)(2)</sup> | 160 |     |     | ps   |
| $t_{h(ADC,A)}$  | Input data hold time on port A after ADCA14 Clk transition   | See <sup>(1)(2)</sup> | 200 |     |     | ps   |
| $t_{su(ADC,B)}$ | Input data setup time on port B before ADCB14 Clk transition | See <sup>(1)(2)</sup> | 180 |     |     | ps   |
| $t_{h(ADC,B)}$  | Input data hold time on port B after ADCB14 Clk transition   | See <sup>(1)(2)</sup> | 220 |     |     | ps   |

- (1) Chip specifications are production tested at 90°C case temperature for the given specification. Early production lots are sample tested at –40°C.
- (2) Setup and hold times apply to data and appropriate ADC Clk, respectively. Timing is measured from ADC Clk threshold crossing.

**Table 20. RX ADC-B7, B14 Switching Characteristics**

| PARAMETER         |                                                              | TEST CONDITIONS       | MIN | NOM | MAX | UNIT |
|-------------------|--------------------------------------------------------------|-----------------------|-----|-----|-----|------|
| $f_{CLK(ADC-AB)}$ | RX input clock frequency, ADCA7 Clk, ADCB7 Clk               | See <sup>(1)</sup>    |     |     | 620 | MHz  |
| $f_{CLK(ADC-C)}$  | RX input clock frequency, ADCC7 Clk                          | See <sup>(1)</sup>    |     |     | 620 | MHz  |
| $t_{su(ADC,A)}$   | Input data setup time on port A before ADCA7 Clk transition  | See <sup>(1)(2)</sup> | 260 |     |     | ps   |
| $t_{h(ADC,A)}$    | Input data hold time on port A after ADCA7 Clk transition    | See <sup>(1)(2)</sup> | 160 |     |     | ps   |
| $t_{su(ADC,B)}$   | Input data setup time on port B before ADCB7 Clk transition  | See <sup>(1)(2)</sup> | 170 |     |     | ps   |
| $t_{h(ADC,B)}$    | Input data hold time on port B after ADCB7 Clk transition    | See <sup>(1)(2)</sup> | 140 |     |     | ps   |
| $t_{su(ADC,C)}$   | Input data setup time on port C before ADCC7 Clk transition  | See <sup>(1)(2)</sup> | 290 |     |     | ps   |
| $t_{h(ADC,C)}$    | Input data hold time on port C after ADCC7 Clk transition    | See <sup>(1)(2)</sup> | 150 |     |     | ps   |
| $t_{su(ADC,A)}$   | Input data setup time on port A before ADCA14 Clk transition | See <sup>(1)(2)</sup> | 130 |     |     | ps   |
| $t_{h(ADC,A)}$    | Input data hold time on port A after ADCA14 Clk transition   | See <sup>(1)(2)</sup> | 200 |     |     | ps   |
| $t_{su(ADC,B)}$   | Input data setup time on port B before ADCB14 Clk transition | See <sup>(1)(2)</sup> | 170 |     |     | ps   |
| $t_{h(ADC,B)}$    | Input data hold time on port B after ADCB14 Clk transition   | See <sup>(1)(2)</sup> | 240 |     |     | ps   |

- (1) Chip specifications are production tested at 90°C case temperature for the given specification. Early production lots are sample tested at –40°C.
- (2) Setup and hold times apply to data and appropriate ADC Clk, respectively. Timing is measured from ADC Clk threshold crossing.


**Figure 21. RX ADC LVDS Timing Specifications (RXA and RXB)**
**Table 21. RXA-BB Switching Characteristics**

| PARAMETER       | TEST CONDITIONS                                            | MIN                   | NOM | MAX | UNIT |
|-----------------|------------------------------------------------------------|-----------------------|-----|-----|------|
| $f_{CLK(BB-A)}$ | RX input clock frequency                                   | See <sup>(1)</sup>    |     | 250 | MHz  |
| $t_{su(BB-A)}$  | Input data setup time on port A before ADCA Clk transition | See <sup>(1)(2)</sup> | 160 |     | ps   |
| $t_{h(BB-A)}$   | Input data hold time on port A after ADCA Clk transition   | See <sup>(1)(2)</sup> | 200 |     | ps   |

- (1) Chip specifications are production tested at 90°C case temperature for the given specification. Early production lots are sample tested at –40°C.
- (2) Setup and hold times apply to data and appropriate ADC Clk, respectively. Timing is measured from ADC Clk threshold crossing.

**Table 22. DPD Clock and Sync A,B Switching Characteristics<sup>(1)</sup>**

| PARAMETER                 | TEST CONDITIONS                                | MIN                | NOM  | MAX          | UNIT |
|---------------------------|------------------------------------------------|--------------------|------|--------------|------|
| $f_{CLK(DPD)}$            | DPD input clock frequency                      | See <sup>(2)</sup> |      | 310<br>{370} | MHz  |
| $f_{CLK(BB)}$             | BB internal clock frequency                    | See <sup>(1)</sup> |      | 250<br>{290} | MHz  |
| $t_{DUTY-CYCLE}$          | DPD input clock duty cycle                     | See <sup>(3)</sup> | 40%  | 60%          |      |
| $f_{CLK (JITTERRMS-DPD)}$ | DPD clock input jitter                         | See <sup>(3)</sup> |      | 2.5%         |      |
| $t_{su(SYNCA)}$           | Input data setup time before $f_{CLK}\uparrow$ | See <sup>(2)</sup> | 0.25 |              | ns   |
| $t_{h(SYNCA)}$            | Input data hold time after $f_{CLK}\uparrow$   | See <sup>(2)</sup> | 0.1  |              | ns   |
| $t_{su(SYNCB)}$           | Input data setup time before $f_{CLK}\uparrow$ | See <sup>(2)</sup> | 0.35 |              | ns   |
| $t_{h(SYNCB)}$            | Input data hold time after $f_{CLK}\uparrow$   | See <sup>(2)</sup> | 0.05 |              | ns   |

- (1) The PLL output ranges are 400–1000 MHz. These are configuration dependent but related to the DPDCLK frequency. The cmd5330 software automatically checks these limits when compiling a configuration.
- (2) Chip specifications are production tested at 90°C case temperature for the given specification. Early production lots are sample tested at –40°C.
- (3) Specification is from the PLL specification and is not production tested.

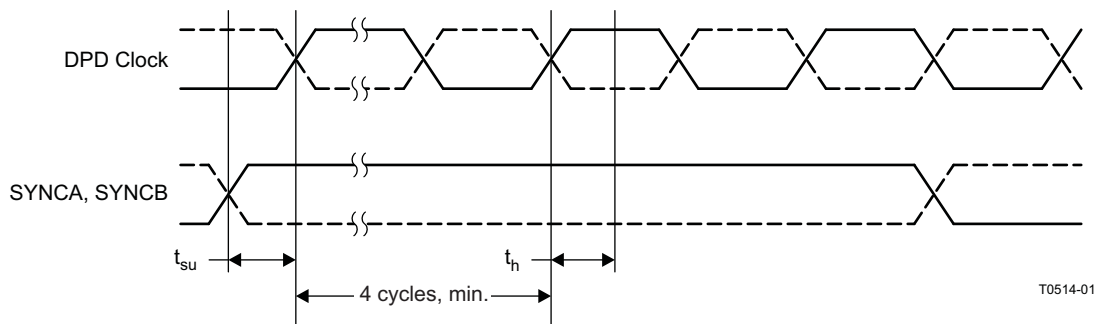


Figure 22. SYNCA, SYNCB Timing to DPD Clock

Table 23. DPD Clock and Sync Out Switching Characteristics

| PARAMETER                | TEST CONDITIONS                      | MIN                | NOM | MAX  | UNIT |
|--------------------------|--------------------------------------|--------------------|-----|------|------|
| $t_{d(\text{SYNCOut})}$  | Data valid after DPD clock           | See <sup>(1)</sup> |     | 0.95 | ns   |
| $t_{HO(\text{SYNCOut})}$ | Data held valid after next DPD clock | See <sup>(1)</sup> |     | 0.3  | ns   |

(1) Chip specifications are production tested at 90°C case temperature for the given specification. Early production lots are sample tested at –40°C.

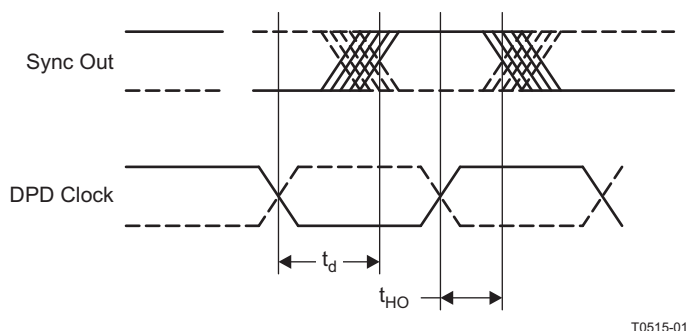


Figure 23. Sync Out Timing to DPD Clock

The JTAG test connections are used with the CMOS signals for board interconnection tests. The TRSTB pin must be toggled low, or low initially. If JTAG is not used, the TRSTB signal should be GROUNDed or tied to GND through < 1 kΩ resistance. TRSTB should be 0 for normal operation.

Table 24. JTAG Switching Characteristics

| PARAMETER                               | TEST CONDITIONS                                        | MIN                | MAX | UNIT |
|-----------------------------------------|--------------------------------------------------------|--------------------|-----|------|
| $f_{\text{TCK}}$                        | JTAG clock frequency                                   |                    | 50  | MHz  |
| $t_{\text{TCKL}}$                       | JTAG clock low period                                  | See <sup>(1)</sup> | 10  | ns   |
| $t_{\text{TCKH}}$                       | JTAG clock high period                                 | See <sup>(1)</sup> | 10  | ns   |
| $t_{\text{su}}(\text{TDI}, \text{TMS})$ | Input data setup time before $f_{\text{TCK}} \uparrow$ | See <sup>(1)</sup> | 7   | ns   |
| $t_{\text{H}}(\text{TDI}, \text{TMS})$  | Input data hold time after $f_{\text{TCK}} \uparrow$   | See <sup>(1)</sup> | 1.5 |      |
| $t_{\text{d}}$                          | Output data delay from $f_{\text{TCK}} \downarrow$     | See <sup>(1)</sup> | 10  | ns   |
| $t_{\text{OHD}}(\text{TDO})$            | Previous data valid from $f_{\text{TCK}} \downarrow$   | See <sup>(1)</sup> | 2   | ns   |

(1) Chip specifications are production tested at 90°C case temperature for the given specification. Early production lots are sample tested at –40°C.

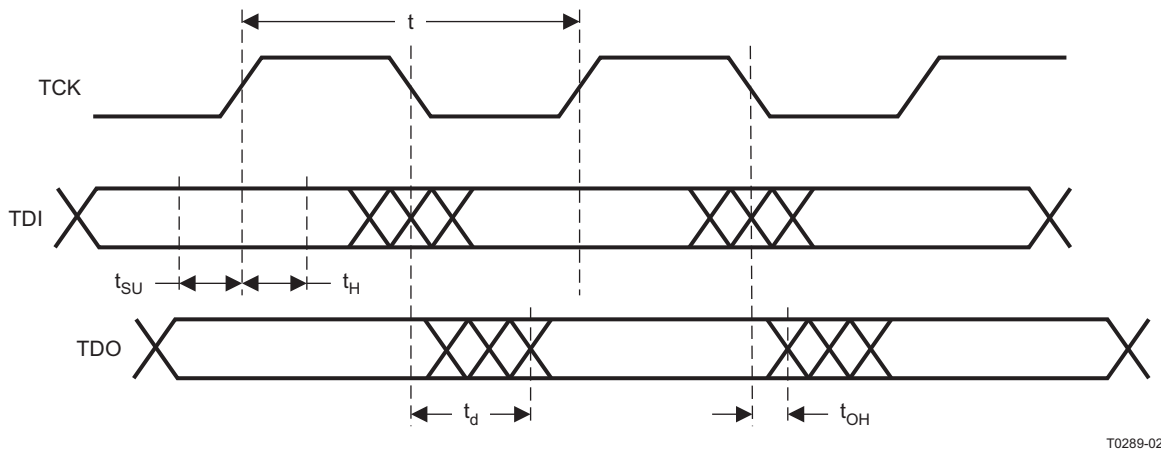


Figure 24. JTAG Timing Specifications

The SPI programming interface is active only when EMIFENA is 0. There are both three-wire and four-wire SPI interfaces; the SPIDO(SPARE) is the fourth wire for SPI data output.

Table 25. SPI Switching Characteristics

| PARAMETER      | TEST CONDITIONS                             | MIN                                        | NOM | MAX | UNIT |
|----------------|---------------------------------------------|--------------------------------------------|-----|-----|------|
| $t_{su(DENB)}$ | Enable setup time before SPI CLK $\uparrow$ | Valid for SPIDENB, see <sup>(1)</sup>      | 5   |     | ns   |
| $t_{su(DI)}$   | Data setup time before SPI CLK $\uparrow$   | Valid for SPIDIO, see <sup>(1)</sup>       | 5   |     | ns   |
| $t_{h(DI)}$    | Input data hold time after CLK $\uparrow$   | Valid for SPIDIO, see <sup>(1)</sup>       | 0.6 |     | ns   |
| $t_{d(DO)}$    | Output data delay from $f_{TCK}\downarrow$  | Valid for SPIDIO, see <sup>(2)</sup>       |     | 8   | ns   |
| $t_{d(DO1)}$   | Output data delay from $f_{TCK}\downarrow$  | Valid for SPIDO(SPARE), see <sup>(2)</sup> |     | 8   | ns   |
| $f_{clk\ SPI}$ | SPI clock frequency                         | See <sup>(1)</sup>                         |     | 50  | MHz  |

- (1) Chip specifications are production tested at 90°C case temperature for the given specification. Early production lots are sample tested at –40°C.
- (2) The SPI data output in three-wire mode comes from SPIDIO; in four-wire mode the output is from SPIDO(SPARE).

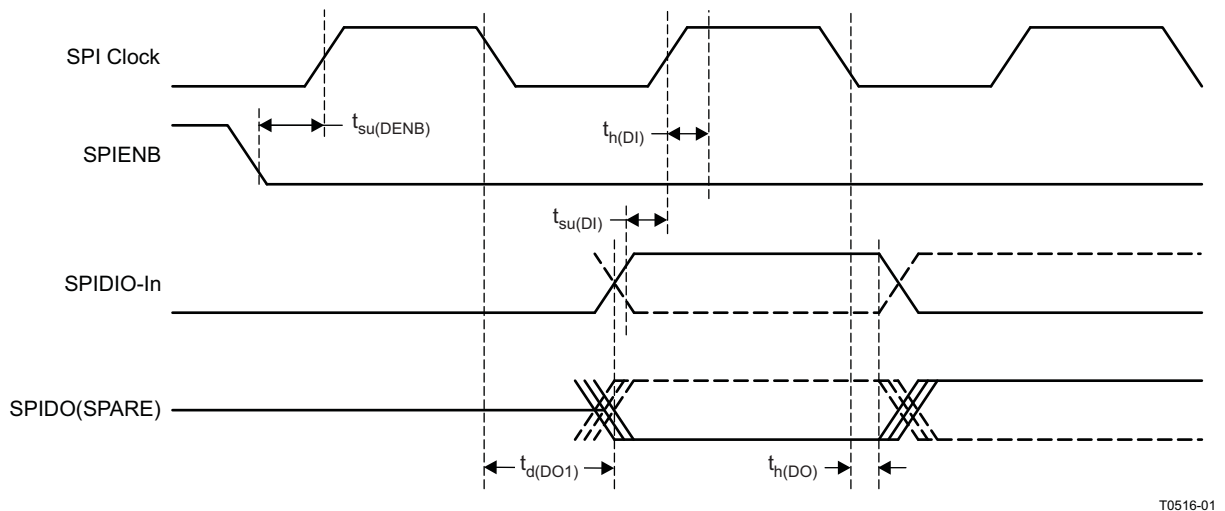


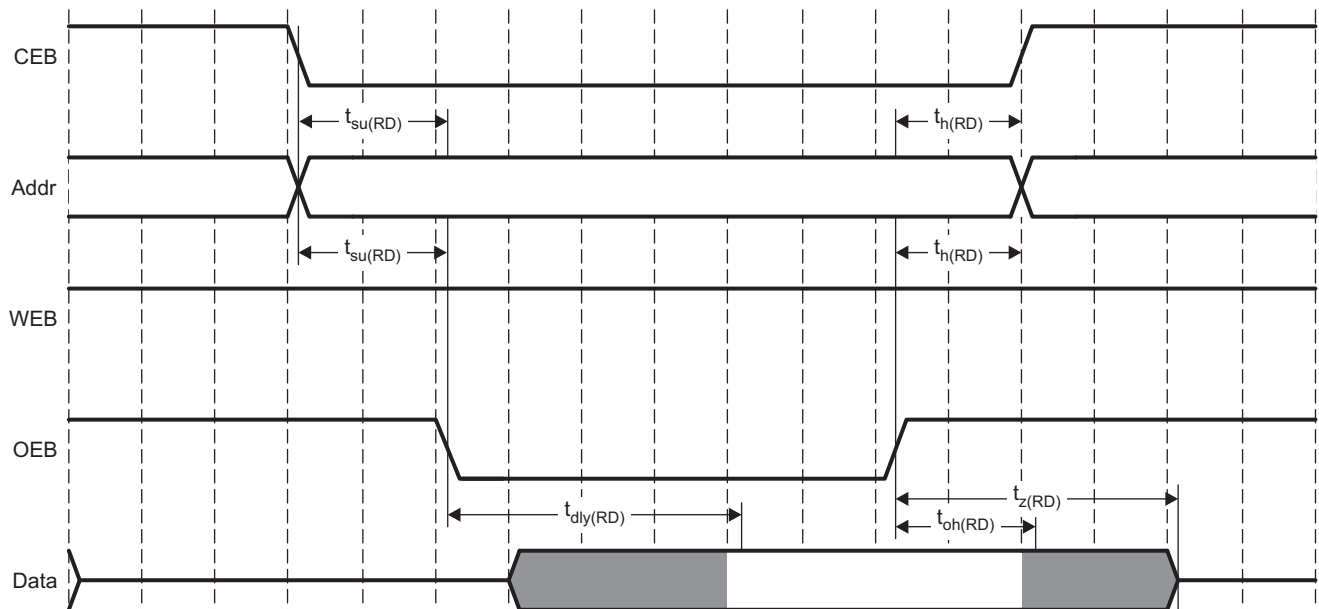
Figure 25. SPI Timing Specifications

**Table 26. MPU Switching Characteristics (READ)**

| PARAMETER       |                                                                          | TEST CONDITIONS    | MIN | MAX | UNIT |
|-----------------|--------------------------------------------------------------------------|--------------------|-----|-----|------|
| $t_{su(RD)}$    | CEB and ADDR setup time to $\downarrow$ OEB                              | See <sup>(1)</sup> | 1.5 |     | ns   |
| $t_{dly(RD)}$   | Data valid time after $\downarrow$ OEB                                   | See <sup>(1)</sup> |     | 15  | ns   |
| $t_{h(RD)}$     | CEB and ADDR hold time to $\uparrow$ OEB                                 | See <sup>(1)</sup> | 2.5 |     | ns   |
| $t_{HIGH(RD)}$  | Time OEB must remain HIGH between READs                                  | See <sup>(1)</sup> | 6   |     | ns   |
| $t_{z(RD)}$     | Data goes to high-impedance state after $\uparrow$ OEB or $\uparrow$ CEB | See <sup>(2)</sup> |     | 5   | ns   |
| $t_{cycle(RD)}$ | Time between READs                                                       | See <sup>(1)</sup> | 21  |     | ns   |
| $t_{oh(RD)}$    | Time after OEB $\uparrow$ that data is valid                             | See <sup>(2)</sup> |     | TBD | ns   |

(1) Chip specifications are production tested at 90°C case temperature for the given specification. Early production lots are sample tested at –40°C.

(2) Bench tested for output start changing after releasing strobe with a 50-Ω load on the output

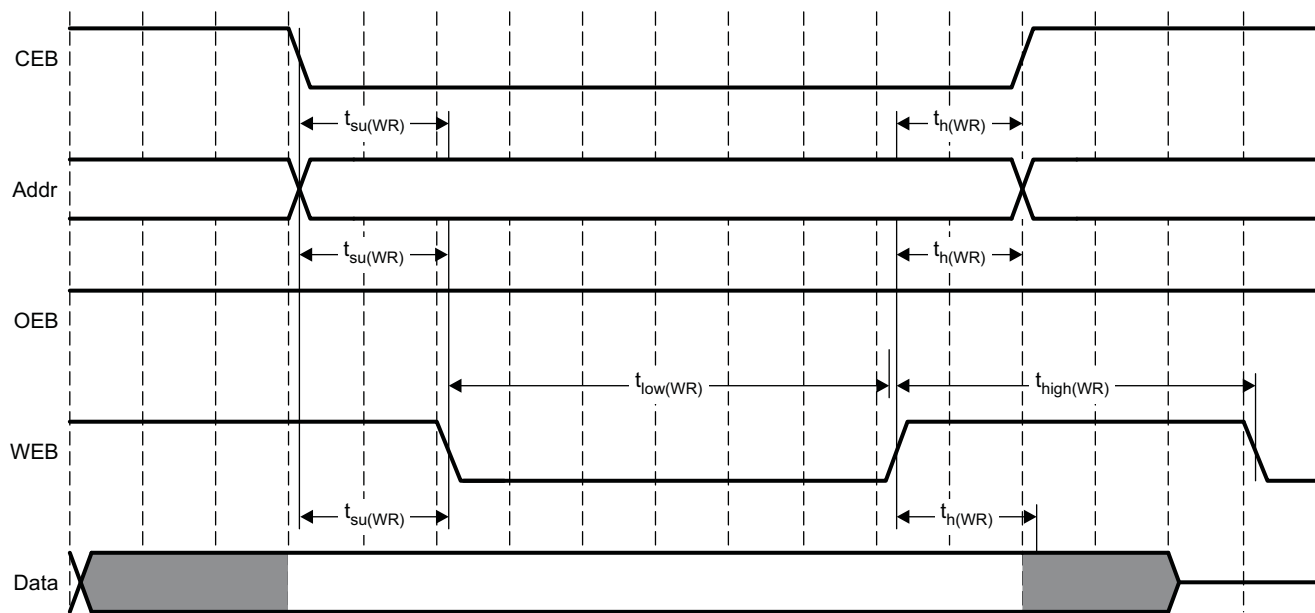


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**Figure 26. MPU READ Timing Specifications****Table 27. MPU Switching Characteristics (WRITE)**

| PARAMETER       |                                                    | TEST CONDITIONS    | MIN | MAX | UNIT |
|-----------------|----------------------------------------------------|--------------------|-----|-----|------|
| $t_{su(WR)}$    | CEB, DATA, and ADDR setup time to $\downarrow$ WEB | See <sup>(1)</sup> | 1.4 |     | ns   |
| $t_{h(WR)}$     | CEB, DATA, and ADDR hold time after $\uparrow$ WEB | See <sup>(1)</sup> | 3   |     | ns   |
| $t_{low(WR)}$   | Time WEB and CEB must remain simultaneously LOW    | See <sup>(1)</sup> | 4   |     | ns   |
| $t_{high(WR)}$  | Time CEB or WRB must remain HIGH between WRITES    | See <sup>(1)</sup> | 7   |     | ns   |
| $t_{cycle(WR)}$ | Time between WRITES                                | See <sup>(1)</sup> | 11  |     | ns   |

(1) Chip specifications are production tested at 90°C case temperature for the given specification. Early production lots are sample tested at –40°C.



T0518-01

**Figure 27. MPU WRITE Timing Specifications**

## Power Sequencing Guideline

TI ASIC I/O design allows either the core supply (VDD) or the I/O supply (VDDS) to be powered up<sup>(2)</sup> for an indefinite period of time while the other power supply is not powered up, if all of these constraints are met:

- Chip is within all maximum ratings and recommended operating conditions.
- Have followed all warnings about exposure to maximum rated and recommended conditions, particularly junction temperature. These apply to power transitions as well as normal operation.
- Bus contention while VDDS is powered up must be limited to 100 hours over the projected lifetime of the device.
- Bus contention while VDDS is powered down may violate the absolute maximum ratings.

However, it is generally good practice to power up VDD, VDDSHV, and VDDS all within 1 second of each other.

## Application Information

The GC533x reference design includes the following additional transmit/receive signal chain components:

- TMS320C6748 digital signal processor (DSP) and DPD adaptation software
- DAC3283 16-bit 800-MSPS, dac348X, or DAC5682 16-bit, 1-GSPS DAC (transmit path)
- CDCE72010 clock generator
- TRF3720 300-MHz to 4.8-GHz quadrature modulator with integrated wideband PLL/VCO
- TRF370317 0.4-GHz to 4-GHz quadrature modulator
- ADS41B49 14-bit, 250-MSPS ADC (and other options; feedback path)
- AMC7823 analog monitoring and control circuit with GPIO and SPI
- PGA870 wideband programmable gain amplifier
- ADS42b49 14-bit dual 250-MSPS receive or complex feedback ADC (and other options; RX path)

## MPU Interface Guidelines

The following section describes the hardware interface between the recommended microprocessor and the GC533x. The GC533x interface is an EMIF asynchronous interface.

(2) A supply bus is powered up when the voltage is within the recommended operating range. It is powered down when it is below that range, either stable or in transition.

The *TMS320C674x/OMAP-L1x Processor Peripherals Overview* reference guide ([SPRUFG9](#)) illustrates the connections to the TMS320C6748 peripherals. The *TMS320C674x/OMAP-L1x Processor External Memory Interface A (EMIFA)* user's guide ([SPRUFL6](#)) illustrates the connections to the EMIF A interface, and DSP timing.

It is recommended that if more than one EMIF-A load is connected to the DSP, buffering is used for the control bus WE, RD, address bus, and data bus.

## Related Material and Documents

The following documents are available through your TI Field Application Engineer FAE:

- GC5330 EVM schematic diagram
- GC5330 EVM layout diagram
- GC533x Baseband Application Note
- GC533x Baseband beAGC Application Note
- GC533x DDUC Application Note
- GC533x CFR Application Note
- GC533x DPD Application Note
- GC533x TX (BUC, DAC Interface) Application Note
- GC533x RX Application Note
- GC533x feAGC Application Note
- GC533x Sync, MPU Application Note
- GC533x Software Application Guide

## APPENDIX

### Glossary of Terms

|         |                                                                                                                    |
|---------|--------------------------------------------------------------------------------------------------------------------|
| 3G      | Third generation (refers to next-generation wideband cellular systems that use CDMA)                               |
| 3GPP    | Third Generation Partnership Project (W-CDMA specification, <a href="http://www.3gpp.org">www.3gpp.org</a> )       |
| 3GPP2   | Third Generation Partnership Project 2 (cdma2000 specification, <a href="http://www.3gpp2.org">www.3gpp2.org</a> ) |
| ACLR    | Adjacent-channel leakage ratio (measure of out-of-band energy from one CDMA carrier)                               |
| ACPR    | Adjacent-channel power ratio                                                                                       |
| ADC     | Analog-to-digital converter                                                                                        |
| BBclk   | Clock-to-baseband section of GC533x                                                                                |
| BW      | Bandwidth                                                                                                          |
| CCDF    | Complementary cumulative distribution function                                                                     |
| CDMA    | Code division multiple access (spread spectrum)                                                                    |
| CEVM    | Composite error vector magnitude                                                                                   |
| CFR     | Crest factor reduction                                                                                             |
| DPD_CLK | Clock-to-DPD section of GC533x                                                                                     |
| CIC     | Cascaded integrator comb (type of digital filter)                                                                  |
| CMOS    | Complementary metal-oxide semiconductor                                                                            |
| DAC     | Digital-to-analog converter                                                                                        |
| dB      | Decibels                                                                                                           |
| dBm     | Decibels relative to 1 mW (30 dBm = 1 W)                                                                           |
| DDR     | Dual data rate (ADC output format)                                                                                 |
| DPD     | Digital pre-distortion                                                                                             |
| DSP     | Digital signal processing or digital signal processor                                                              |
| DUC     | Digital upconverter (usually provides the GC533x input)                                                            |
| EVM     | Error vector magnitude                                                                                             |
| FIR     | Finite impulse response (type of digital filter)                                                                   |
| HP-DPD  | High-performance DPD mode of the GC533x                                                                            |
| HS-DPD  | High-speed DPD mode of the GC533x                                                                                  |
| I/Q     | In-phase and quadrature (signal representation)                                                                    |
| IF      | Intermediate frequency                                                                                             |
| IIR     | Infinite impulse response (type of digital filter)                                                                 |
| JTAG    | Joint Test Action Group (chip debug and test standard 1149.1)                                                      |
| LO      | Local oscillator                                                                                                   |
| LSB     | Least-significant bit                                                                                              |
| MSB     | Most-significant bit                                                                                               |
| MSPS    | Megasamples per second ( $1 \times 10^6$ samples/s)                                                                |
| PA      | Power amplifier                                                                                                    |
| PAR     | Peak-to-average ratio                                                                                              |
| PCDE    | Peak code domain error                                                                                             |
| PDC     | Peak detection and cancellation (stage)                                                                            |
| PDF     | Probability density function                                                                                       |
| RF      | Radio frequency                                                                                                    |
| RMS     | Root-mean-square (method to quantify error)                                                                        |
| SDR     | Single data rate (ADC output format)                                                                               |
| SEM     | Spectrum emission mask                                                                                             |
| SNR     | Signal-to-noise ratio (usually measured in dB or dBm)                                                              |
| UMTS    | Universal mobile telephone service                                                                                 |
| W-CDMA  | Wideband code division multiple access (synonymous with 3GPP)                                                      |

|       |                                                               |
|-------|---------------------------------------------------------------|
| WiBro | Wireless Broadband (Korean initiative IEEE 802.16e)           |
| WiMAX | Worldwide Interoperability of Microwave Access (IEEE 802.16e) |

## REVISION HISTORY

| Changes from Revision A (December 2010) to Revision B                                          | Page |
|------------------------------------------------------------------------------------------------|------|
| • Revised GC533x block diagram .....                                                           | 7    |
| • Added text in next-to-last paragraph of <a href="#">Input and Output Syncs</a> section ..... | 28   |
| • Combined GC5330 and {GC5337} values into a single row in <a href="#">Table 22</a> .....      | 39   |
| • Revised <a href="#">Figure 22</a> .....                                                      | 40   |
| • Revised <a href="#">Figure 25</a> .....                                                      | 41   |

## PACKAGING INFORMATION

| Orderable Device | Status<br>(1) | Package Type | Package<br>Drawing | Pins | Package<br>Qty | Eco Plan<br>(2)            | Lead/Ball Finish<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5)   | Samples |
|------------------|---------------|--------------|--------------------|------|----------------|----------------------------|-------------------------|----------------------|--------------|---------------------------|---------|
| GC5330IZEV       | NRND          | BGA          | ZEV                | 484  | 60             | Green (RoHS<br>& no Sb/Br) | SNAGCU                  | Level-3-260C-168 HR  | -40 to 85    | GC5330IZEV<br>DIGITAL TRX |         |
| GC5337IZEV       | NRND          | BGA          | ZEV                | 484  | 60             | Green (RoHS<br>& no Sb/Br) | SNAGCU                  | Level-3-260C-168 HR  | -40 to 85    | GC5337IZEV<br>DIGITAL TRX |         |

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

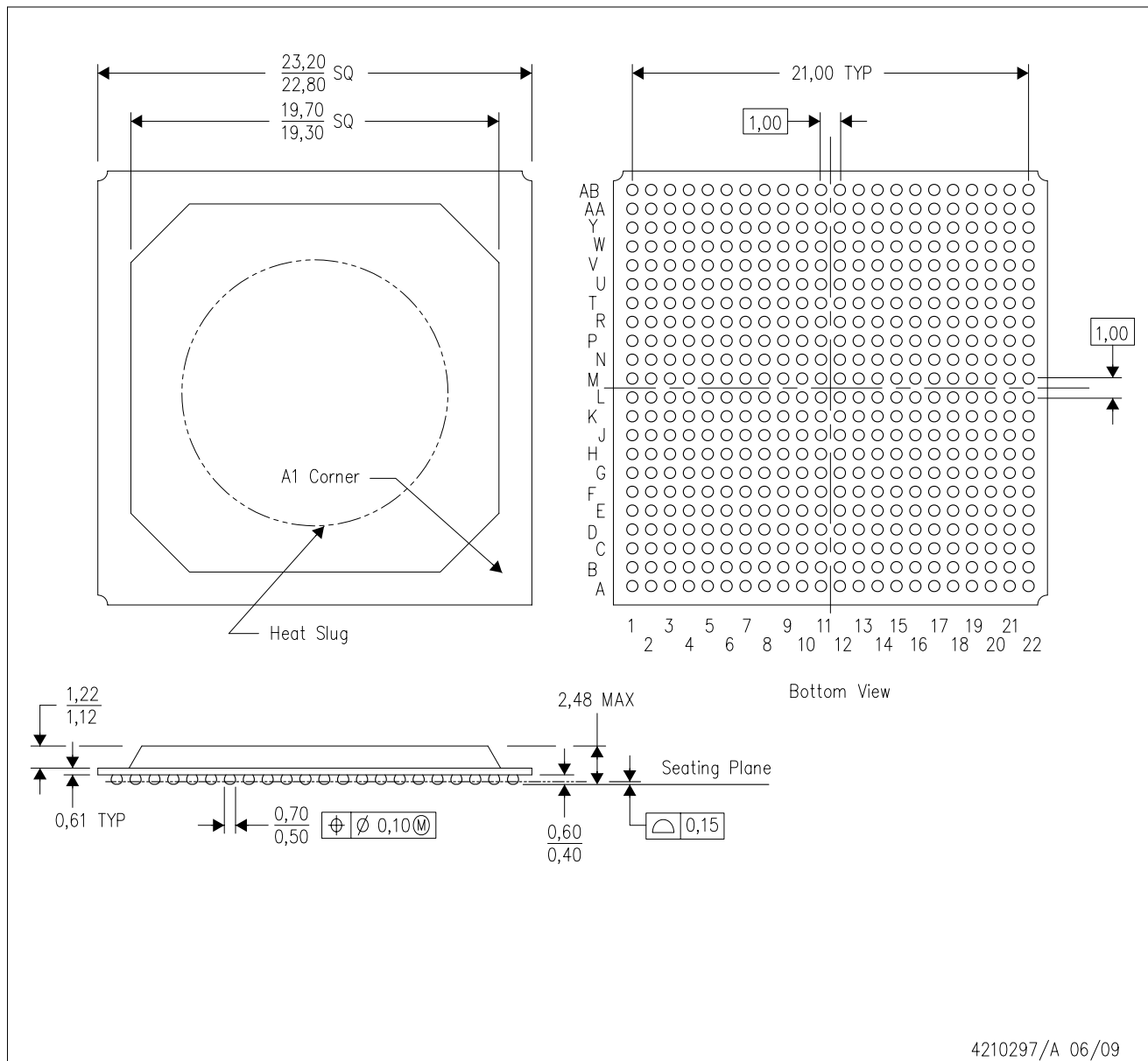
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ZEV (S-PBGA-N484)

PLASTIC BALL GRID ARRAY



- NOTES:
- All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - This drawing is subject to change without notice.
  - Falls within JEDEC MO-151
  - Thermally enhanced molded plastic package with heat slug (HSL) and embedded thermal spacer.
  - This package is Pb-free.

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